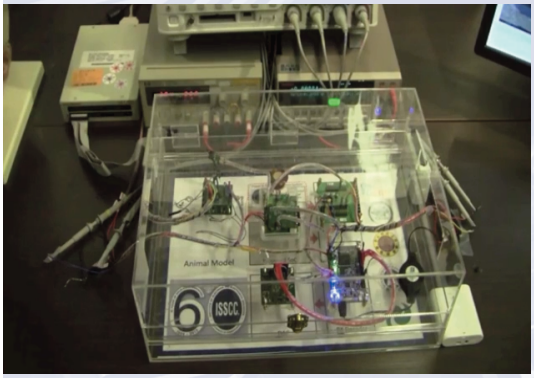
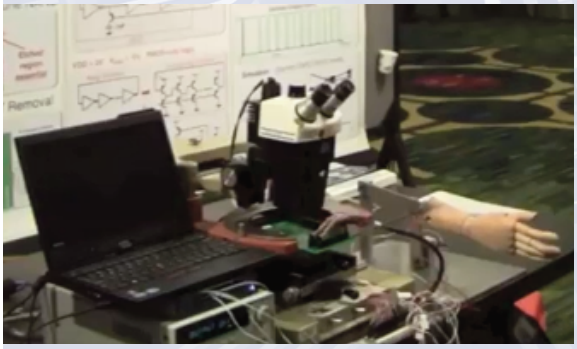
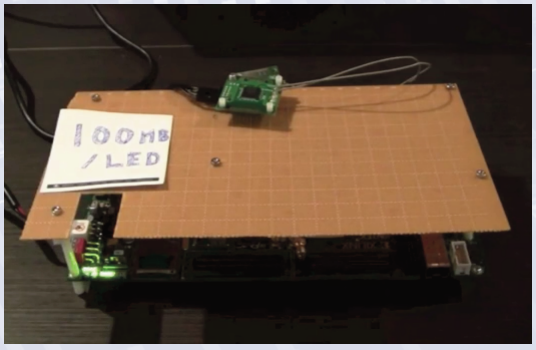
ISSCC 2014 Demonstration Session

Monday February 10, 2014: 400 pm - 7:00 pm

(Golden Gate Hall)







ISSCC 2014 Demonstration Session Welcome

What is an ISSCC Demonstration Session?

Demonstration sessions are designed to augment the experience of all attendees by providing an opportunity for direct interaction with authors of selected papers and view some of their concrete results. At their demonstration, the authors will illustrate their research results face-to-face, providing attendees with a more hands-on experience.

Overall, these Sessions will:

- Demonstrate chip operation.
- Provide opportunity for in-depth discussion with the chip creators.

The Demonstration Session will be held on Monday, February 10 from 4 to 7 pm in the Golden Gate Hall.

As well, these demonstrations will be recorded and posted at www.isscc.org after the Conference.

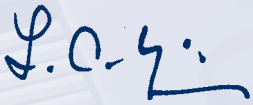
Acknowledgements:

In the preparation of these demonstration sessions, I wish to first acknowledge the authors of the participating papers. Their work has been organized and structured under the joint Chairmanship of **Bill Bowhill** (Intel) and **Uming Ko** (MediaTek), and the Demonstration Session Committee, consisting of: **Roman Genov** (University of Toronto), **Tetsuya Iizuka** (University of Tokyo), **Chewnpu Jou** (TSMC), **Tae-Chan Kim** (Samsung), **Li Lin** (Marvell Semiconductor), **Saska Lindfors** (Texas Instruments), Masaitsu Nakajima (Panasonic), **Byeong-Gyu Nam** (Chungnam National University), **Tobias Noll** (RWTH Aachen University), **Ahmad Mirzaei** (Pennsylvannia State University), **Yongha Park** (Samsung), **Pirooz Parvarandeh** ((Maxim), and **Takefumi Yoshikawa** (Panasonic),

Further, I wish to recognize **Dave Hulupka** (Kapik), and a group of volunteer-graduate students from the University of Toronto for their videography; as well, **Brad Phillips, Alija Husic** (Mira Digital Publishing) and **Steve Bonney** (S3 Digital Publishing) for the structuring and formatting of this handout, and the tablet version (available for download from ISSCC 2014).

Finally, I would like to acknowledge the vision and encouragement of the ISSCC Conference Chair, **Anantha Chandrakasan** (MIT), for his leadership in the realization of the demonstration-session idea.

Enjoy!



Laura Chizuko Fujino

ISSCC Director of Publications & Presentations

lcfujino@aol.com

February 2014

ISSCC 2014 Demonstration Session Papers

Paper 1.3: **How Chips Pave the Road to the Higgs Particle and the Attoworld Beyond**

Erik H. M. Heijne,
Instrumentation Physicist, CERN PH Department, Geneva, Switzerland also with IEAP Czech Technical University Prague & Nikhef Amsterdam

Paper 2.1: **28Gb/s 560mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision-Feedback Equalizer in 28nm CMOS**

Hiroshi Kimura, Pervez Aziz, Tai Jing, Ashutosh Sinha, Ram Narayan, Hairong Gao, Ping Jing, Gary Hom, Anshi Liang, Eric Zhang, Aniket Kadkol, Ruchi Kothari, Gordon Chan, Yehui Sun, Benjamin Ge, Jason Zeng, Kathy Ling, Michael Wang, Amaresh Malipatil, Shiva Kotagiri, Lijun Li, Chris Abel, Freeman Zhong
LSI, San Jose, CA

Paper 5.4: **Ivytown: A 22nm 15-Core Enterprise Xeon® Processor Family**

Jim Guzzo, Stefan Rusu, Harry Muljono, David Ayers, Simon Tam, Wei Chen, Aaron Martin, Shenggao Li, Sujal Vora, Raj Varada, Eddie Wang
Intel, Santa Clara, CA

Paper 5.9 and 13.1: **Haswell: A Family of IA 22nm Processors**

C. Honl, D. Sutherland, F. Hamzaoglu, N. Kurd, M. Chowdhury, E. Burton, T.P. Thomas, C. Mozak, B. Boswell, M. Lal, A. Deval, J. Douglas, M. Elassal, A. Nalamalpu, T.M., Wilson, M. Merten, S. Chennupaty, W. Gomes, R. Kumar, U. Arslan, N. Bisnik, S. Ghosh, M. B. Lal, N. Lindert, M. Meterelliyoz, R.B. Osborne, J. Park, S. Tomishima, Y. Wang, K. Zhang
Intel, Hillsboro, OR

Paper 7.6: **A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC**

Andrew Payne, Andy Daniel, Anik Mehta, Barry Thompson, Cyrus S. Bamji, Dane Snow, Hideaki Oshima, Larry Prather, Mike Fenton, Lou Kordus, Pat O'Connor, Rich McCauley, Sheethal Nayak, Sunil Acharya, Swati Mehta, Tamer Elkhatib, Thomas Meyer, Tod O'Dwyer, Travis Perry, Vei-Han Chan, Vincent Wong, Vishali Mogallapu, William Qian, Zhanping Xu
Microsoft, Mountain View, CA

Paper 8.2: **A 12×5 Two-Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS**

Hiroshi Morita, Koki Uchino, Eiji Otani, Hiizu Ohtorii, Takeshi Ogura, Kazunao Oniki, Shuichi Oka, Shusaku Yanagawa, Hideyuki Suzuki
Sony, Tokyo, Japan

Paper 9.1: **A Self-Calibrating NFC SoC with a Triple-Mode Reconfigurable PLL and a Single-Path PICC-PCD Receiver in 0.11µm CMOS**

Wee Liang Lien[1], Tieng Ying Choke[1], Ying Chow Tan[1], Ming Kong[1], Eng Chuan Low[1], Dan Ping Li[1], Liming Jin[1], Huajiang Zhang[1], Chin Heng Leow[1], Soong Lin Chew[1], Uday Dasgupta[1], Chee Hong Yong[1], Tian Bao Gao[1], Geok Teng Ong[1], Wee Guan Tan[1], Weimin Shu[1],Chee Lee Heng[1], Osama Shana'A[1,2]
[1]MediaTek, Singapore, Singapore,
[2]MediaTek, San Jose, CA

Paper 9.7: **A 0.33nJ/b IEEE802.15.6/Proprietary-MICS/ISM-Band Transceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications**

Maja Vidojkovic[1], Xiongchuan Huang[1], Xiaoyan Wang[1], Cui Zhou[1], Ao Ba[1], Maarten Lont[1], Yao-Hong Liu[1], Pieter Harpe[2], Ming Ding[1], Ben Busze[1], Nauman Kiyani[1], Kouichi Kanda[3], Shoichi Masui[3], Kathleen Philips[1], Harmke de Groot[1]
[1]Holst Centre/imec, Eindhoven, The Netherlands, [2]Eindhoven University of Technology, Eindhoven, The Netherlands,
[3]Fujitsu Laboratories, Kawasaki, Japan

Paper 10.7: **A 105GOPS 36mm² Heterogeneous SDR MPSoC with Energy-Aware Dynamic Scheduling and Iterative Detection-Decoding for 4G in 65nm CMOS**

Benedikt Noethen, Oliver Arnold, Esther Pérez Adeva, Tobias Seifert Erik Fischer, Steffen Kunze, Emil Matúš, Gerhard Fettweis, Holger Eisenreich, Georg Ellguth, Stephan Hartmann, Sebastian Höppner, Stefan Schiefer, Jens-Uwe Schlüßler, Stefan Scholze, Dennis Walter, René Schüffny
Technische Universität Dresden, Dresden, Germany

Paper 11.3: **A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation**

Frank M. Yaul, Anantha P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

Paper 12.1: **3D Ultrasonic Gesture Recognition**

Richard J. Przybyla[1], Hao-Yen Tang[1], Stefon E. Shelton[2], David A. Horsley[2], Bernhard E. Boser[1]
[1]University of California, Berkeley, CA, [2]University of California, Davis, CA

Paper 12.2: **3D Gesture-Sensing System for Interactive Displays Based on Extended-Range Capacitive Sensing**

Yingzhe Hu, Liechao Huang, Warren Rieutort-Louis, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma
Princeton University, Princeton, NJ

Paper 12.3: **A 240Hz-Reporting-Rate 143×81 Mutual-Capacitance Touch-Sensing Analog Front-End IC with 37dB SNR for 1mm-Diameter Stylus**

Mutsumi Hamaguchi[1], Akira Nagao[2], Masayuki Miyamoto[2]
[1]Sharp, Fukuyama, Japan, [2]Sharp, Tenri, Japan

ISSCC 2014 Demonstration Session Papers

Paper 12.4: **A 1mm-Pitch 80×80-Channel 322Hz-Frame-Rate Touch Sensor with Two-Step Dual-Mode Capacitance Scan**

Noriyuki Miura[1], Shiro Dosho[2], Satoshi Takaya[1], Daisuke Fujimoto[1], Takumi Kiriyama[1], Hiroyuki Tezuka[2], Takuji Miki[2], Hiroto Yanagawa[2], Makoto Nagata[1]

[1]Kobe University, Kobe, Japan, [2]Panasonic, Osaka, Japan

Paper 12.8: **A BJT-Based CMOS Temperature Sensor with a 3.6pJ·K2-Resolution FoM**

Ali Heidary[1,2,3], Guijie Wang[1,2], Kofi Makinwa[2], Gerard Meijer[1,2,4]

[1]Smartec, Breda, The Netherlands, [2]Delft University of Technology, Delft, The Netherlands, [3]Guilan University, Rasht, Iran, [4]SensArt, Delft, The Netherlands

Paper 14.5: **A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13µm SiGe BiCMOS**

Ullrich R Pfeiffer[1], Yan Zhao[1], Janusz Grzyb[1], Richard Al Hadi[1], Neelanjan Sarmah[1], Wolfgang Förster[1], Holger Rücker[2], Bernd Heinemann[2]

[1]University of Wuppertal, Wuppertal, Germany, [2]IHP, Frankfurt (Oder), Germany

Paper 16.1 and 5.7: **Energy-efficient Circuit Techniques for Networks-on-Chip and Graphics**

G. Chen, C. Tokunaga, M. A. Anders, J. Ryan, H. Kaul, C. Augustine, S. K. Satpathy, J. Kulkarni, S. K. Mathew, Y.C. Shih, S. K. Hsu, S. Kim, A. Agarwal, R. Jain, K. Bowman, A. Raychowdhury, M. Khellah, R.K. Krishnamurthy, J. Tschanz, S. Borkar, V. De

Intel, Hillsboro, OR

Paper 17.4: **CMOS Impedance Analyzer for Nanosamples Investigation Operating up to 150MHz with Sub-aF Resolution**

Giorgio Ferrari, Davide Bianchi, Angelo Rottigni, Marco Sampietro

Politecnico di Milano, Milan, Italy

Paper 18.1: **A 1V 3mA 2.4GHz Wireless Digital Audio Communication SoC for Hearing-Aid Applications in 0.18µm CMOS**

Amre El-Hoiydi[1], François Callias[1], Yves Oesch[1],Christoph Kuratli[2], Robert Kvacek[3]

[1]Phonak Communications, Murten, Switzerland, [2]EM Microelectronic, Marin, Switzerland, [3]ASICentrum, Prague, Czech Republic

Paper 18.2: **A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18µm HVCMOS**

Marcus Yip[1], Rui Jin[1], Nathan Ickes[1], Hideko Heidi Nakajima[2,3], Konstantina M. Stankovic[2,3], Anantha P. Chandrakasan[1]

[1]Massachusetts Institute of Technology, Cambridge, MA, [2]Harvard Medical School, Boston, MA, [3]Massachusetts Eye and Ear Infirmary, Boston, MA

Paper 18.3 and 10.6: **Biomedical Wireless Sensor Platform Comprising Multi-Parameter Signal Acquisition SoC and 2.4 GHz Bluetooth Smart / Zigbee / IEEE 802.15.6 Personal Area Networks Radio**

C. Bachmann[2], G. van Schaik[2], B. Busze[2], M. Konijnenburg[2], Y. Zhang[2], J. Stuyt[2], M. Ashouei[2], G. Dolmans[2], T. Gemmeke[2], H. de Groot[2], N. Van Helleputte[2], M. Konijnenburg[2], H. Kim[1],J. Pettine[1], D.W. Jee[1], A. Breeschoten[2], A. Morgado[1],T. Torfs[1], R. F. Yazicioglu[1], C. Van Hoof[1]

[1]imec, Leuven, Belgium, [2]Holst Centre/imec, Eindhoven, The Netherlands

Paper 20.5: **A 40nm Dual-Band 3-Stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s Over-the-Air Throughput**

Ming He, Renaldi Winoto, Xiang Gao, Wayne Loeb, David Signoff, Wai Lau, Yuan Lu, Donghong Cui, Kun-Seok Lee, Sai-Wang Tam, Philip Godoy, Yung Chen, Sanghoon Joo, Changhui Hu, Arvind Anumula Paramanandam, Xiaoyue Wang, Chi-Hung Lin, Li Lin

Marvell, Santa Clara, CA

Paper 22.5: **A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS**

Nicolas Le Dortz[1,2], Jean-Pierre Blanc[1], Thierry Simon[1], Sarah Verhaeren[1], Emmanuel Rouat[1], Pascal Urard[1], Stéphane Le Tual[1], Dimitri Goguet[1], Caroline Lelandais-Perrault[2], Philippe Benabes[2]

[1]STMicroelectronics, Crolles, France, [2]Supélec, Gif-sur-Yvette, France

Paper 26.2: **A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS**

James Jaussi[1], Ganesh Balamurugan[1], Sami Hyvonen[1], Tzu-Chien Hsueh[1], Tawfiq Musah[1], Gokce Keskin[1], Sudip Shekhar[1,], Joseph Kennedy[1], Shreyas Sen[1], Rajesh Inti[1], Mozhgan Mansuri[1], Michael Leddige[1], Bryce Horine[1], Clark Roberts[1], Randy Mooney[2], Bryan Casper[1]*

[1]Intel, Hillsboro, OR, [2]Intel, Mapleton, UT, *now with University of British Columbia, Vancouver, Canada

Paper 26.3: **A Pin- and Power-Efficient Low-Latency 8-to-12Gb/s/wire 8b8w-Coded SerDes Link for High-Loss Channels in 40nm Technology**

Anant Singh[1], Dario Carnelli[1], Altay Falay[1], Klaas Hofstra[1], Fabio Licciardello[1], Kia Salimi[1], Hugo Santos[1], Amin Shokrollahi[1], Roger Ulrich[1], Christoph Walter[1], John Fox[2], Peter Hunt[2], John Keay[2], Richard Simpson[2], Andy Stewart[2], Giuseppe Surace[2], Harm Cronie[3]

[1]Kandou Bus, Lausanne, Switzerland, [2]Kandou Bus, Northampton, United Kingdom, [3]Lausanne, Switzerland

Paper 30.2: **Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption**

Jan Genoe[1,2], Koji Obata[3], Marc Ameys[1], Kris Myny[1], Tung Huei Ke[1], Manoj Nag[1], Soeren Steudel[1], Sarah Schols[1], Joris Maas[4],Ashutosh Tripathi[4], Jan-Laurens van der Steen[4], Tim Ellis[4],Gerwin H. Gelinck[4], Paul Heremans[1,2,4]

[1]imec, Leuven, Belgium, [2]KU Leuven, Leuven, Belgium, [3]Panasonic, Osaka, Japan, [4]Holst Centre/TNO, Eindhoven, The Netherlands

Paper No. : 1.3

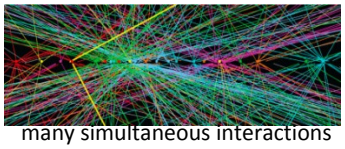
How Chips Pave the Road to the Higgs Particle and the Attoworld Beyond
Imaging of trails of particles/ energy quanta with pixelized 2-layer Si + CMOS Timepix chip

Erik H.M. Heijne CERN PH Department CH 1211 Genève 23
Institute for Experimental and Applied Physics of the Czech Technical University in Prague
Nikhef Amsterdam

Motivation

Reconstruction of interactions of TeV protons in the CERN Large Hadron Collider experiments need fast (ns) and precise (µm) detectors that can record coordinates of many particles simultaneously. 3-D pixel detectors have been developed and in the central region of the experiments several m² of these devices have been deployed. These prove essential for mastering the extreme radiation environment, and they resolve particle tracks from interactions at the 40MHz rate.

pixel detector array under construction

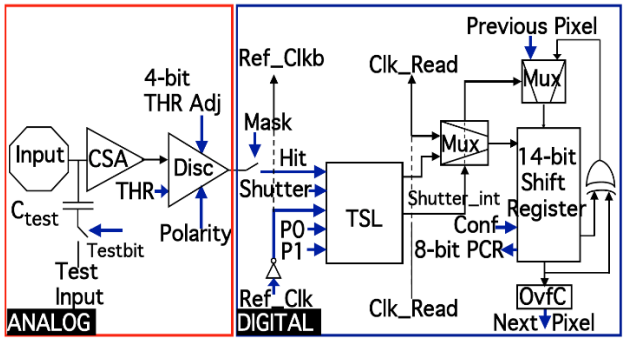


many simultaneous interactions in one collision of the two beams

As a spin-off, the Timepix hybrid, 2-layer assembly of sensor and CMOS readout chip is a quantum imager, using similar concepts, including more sophisticated circuitry. A variety of scientific applications is possible. In time-of-flight mode, for example, laser-evaporated biological molecules can be imaged and identified.

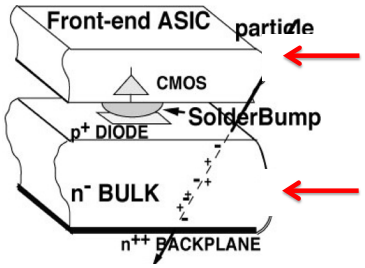
Architecture

Schematic Block Diagram of pixel Timepix chip



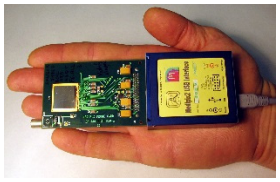
Matrix has 256x256 pixels, of 55µmx55µm
Typical input signal is 1000 to 100k electrons
Charge sensitive amplifier CSA is followed by comparator with adjustable threshold
Signal can be digitized by counting clock pulses during Time-over-Threshold ToT
Globally distributed Clock can be 1MHz-100MHz
Counting also can be used to determine arrival time of pulse and Time-of-Flight
Exposure time window can be adjusted with ns precision from 0.1µs to hours

System Implementation

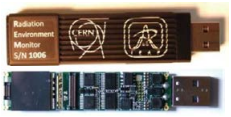


Readout matrix!
!
Pixel size 50µmx50µm!
Typical 256x256!
!
Sensor matrix!

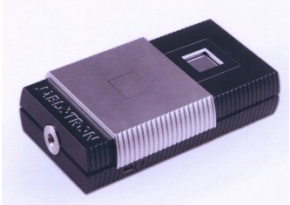
Chip, sensor & support ICs
on printed circuit board: DC bias, FPGA, driver
USB box



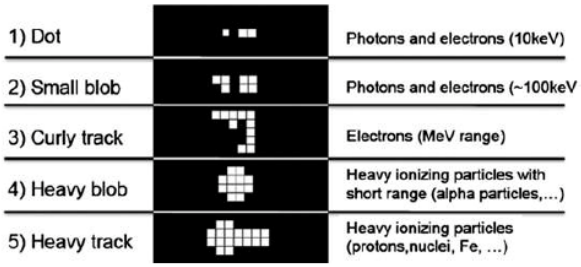
USB Lite



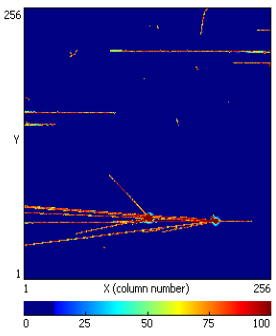
Educational Unit



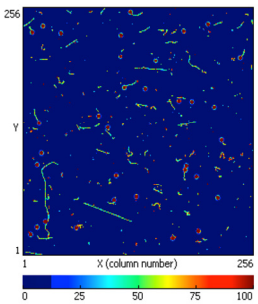
Verification



A particle/energy quantum generates a typical cluster of pixels, which allows identification and 'quantum' dosimetry



Timepix in GeV pion beam incident from right side



Timepix at home images Radon decays

Paper No. : 2.1

28Gb/s 560mW Multi-Standard SerDes with Single Stage Analog-Front End and 14-tap Decision Feedback Equalizer in 28nm CMOS

Hiroshi Kimura, Pervez Aziz, Tai Jing, Ashutosh Sinha, Ram Narayan, Hairong Gao, Ping Jing, Shiva Kotagiri, Amaresh Malipatil, Gary Hom, Anshi Liang, Aniket Kadkol, Eric Zhang, Gordon Chan, Ruchi Kothari, Kathy Ling, Yehui Sun, Benjamin Ge, Jason Zeng, Michael Wang, Chris Abel, Freeman Zhong / LSI

Motivation

•New Standard require 25~28Gbps data rate.

OIF CEI-25G-LR, CEI-28G-MR/SR/VSR, IEEE802.3bj and 32G-FC

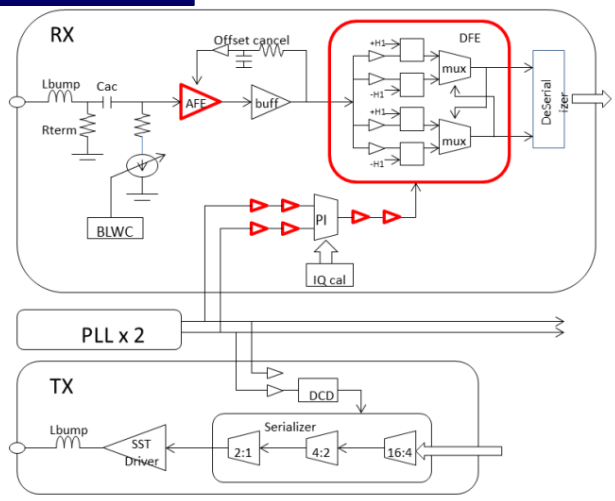
•High Speed Serdes challenges.

-High speed operation.
-Low power consumption.
-Small die area.
-Intensive equalization
-Robustness.

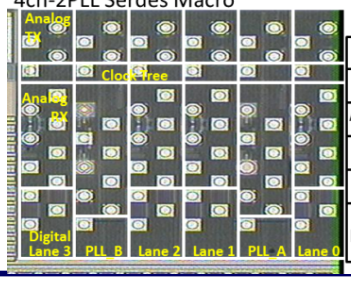
•Needs for new circuit topology and system architecture.

-TIA base single stage AFE with compact inductor.
-Unrolled DFE with two error latch.
-Two stage sense amplifier slicer with 15mV sensitivity.
-Low power active inductor buffer.

Architecture



4ch-2PLL Serdes Macro

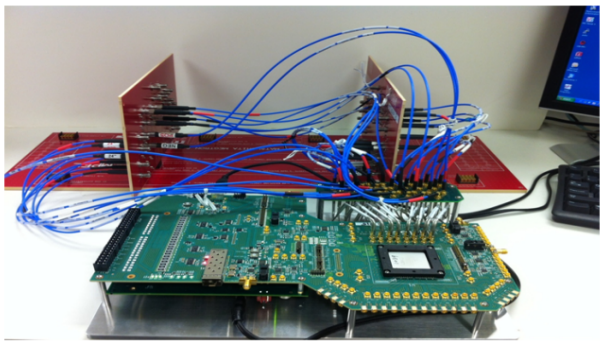


Transceiver Summary Table

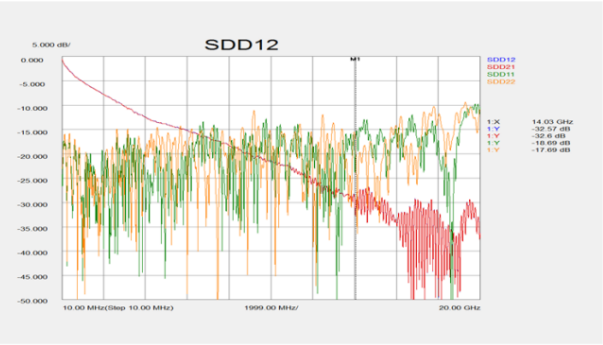
Technology	28nm CMOS
Power Supply	1.5V / 1.05V / 0.85V
Area (4 channel+2 pll)	3.34 mm2
Data Rate Range	1.25 ~ 28.5 Gbps
Channel Loss	30dB @ 14GHz
Measured Worst Power Consumption	560 mW 3 sigma ff corner,temp=125

System Implementation

• Test setup: 4 X 25.78125Gb/s over Molex backplane with PRBS31 traffics



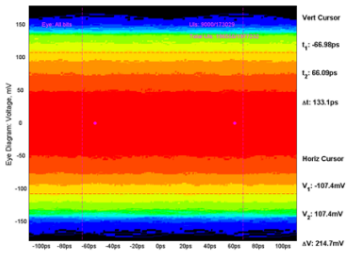
• Measured channel insertion loss: 32.6dB at 14GHz



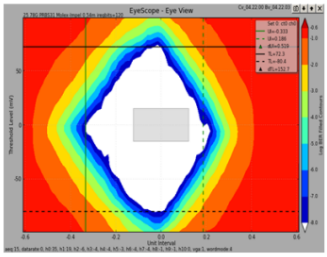
Verification

• Demonstrate error-free operation with sufficient performance margin: VM = 153mVdpp, HM = 0.52UI

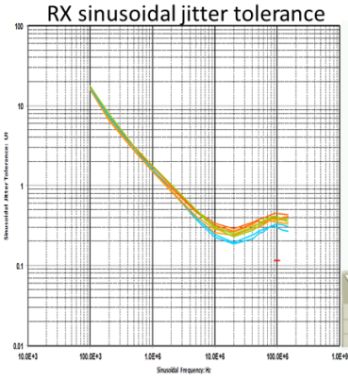
Received eye at receiver



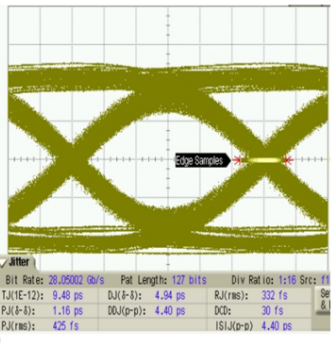
Equalized eye



100G Ethernet
RX sinusoidal jitter tolerance



TX eye diagram of 28G PRBS7



Paper No. : 5.4

Ivytown: A 22nm Xeon® Processor

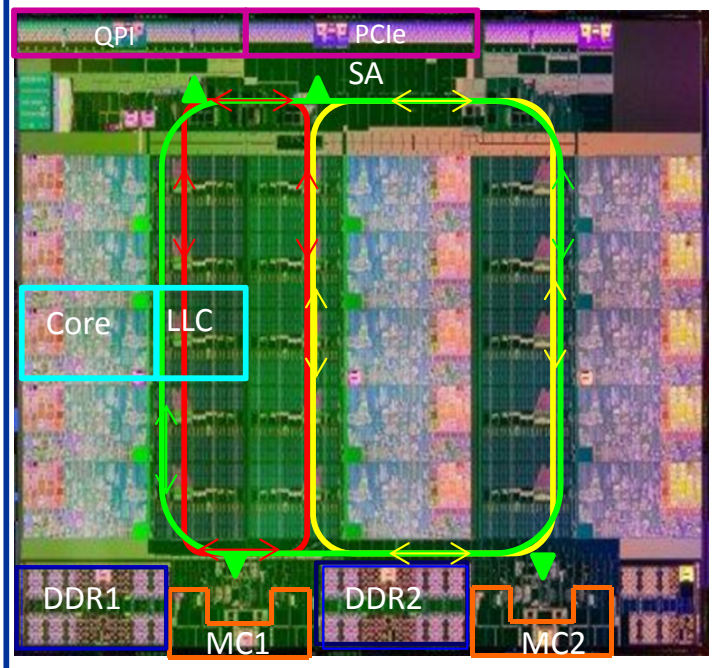
James Guzzo, Stefan Rusu, Harry Muljono, David Ayers, Simon Tam, Wei Chen,
Aaron Martin, Shenggao Li, Sujal Vora, Raj Varada, Eddie Wang
Intel, Santa Clara, CA

Motivation

High Level Goals
Intel® Xeon® Processor E5-2600 v2 Product Family

- **Delivers More Computing, Flexibility for Next Generation of Datacenters.**
  - Family of 22 nm processors ideally suited for high performance computing, cloud and enterprise segments, and offer compelling new opportunities for telecommunications
- **Enable up to 50%[1] more performance**
  - 1.5X increase in core count and cache size going from 8 Cores / 16T/20MB to 12 Cores/ 24T/ 30MB LLC using Intel's 22nm Tri-gate process.
  - Scalable concentric Ring architecture for matched uncore bandwidth.
  - 33% increase in memory bandwidth through dual memory controllers supporting increased memory speeds (from 1600 to 1866 DDR3)
  - Deliver across the 50W to 150W TDP Sku range
- **Offers up to 45%[2] greater efficiency**

Architecture



System Implementation

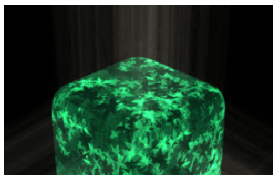
System 1 – 32nm

System 2 -22nm

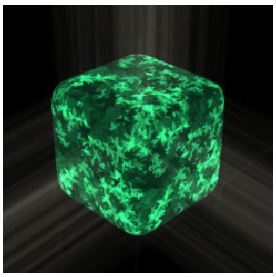
• Liquid Cooled Intel GZ2600 EP platform	• Liquid Cooled Intel GZ2600 EP platform
• 2 Intel Xeon E5 2680 – 2.7GHz/20MB/8C – 130W TDP – 32nm Previous gen	• 2 Intel Xeon E5 2697 V2 – 2.7GHz/30MB/12C – 130W TDP – 22nm Current gen
• 128GB 1600MHz DDR3	• 128GB 1866MHz DDR3
• Two 480GB Intel 520 Series sata SSD	• Two 480GB Intel 520 Series sata SSD

Verification

- Both Systems Running Windows* 7 Enterprise SP1
- Both Systems Rendering Identical Images
  - using POV-Ray v3.7 Beta



System 1 32 Threads

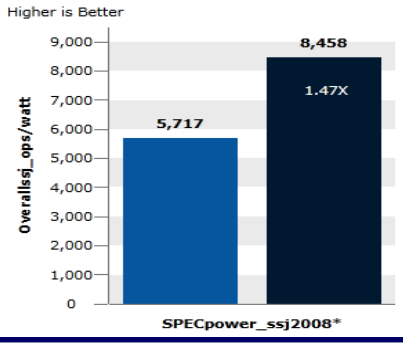


System 2 48 Threads

- **Energy efficiency**

System Idle procesor power

Sys1 = 30 W
Sys2 = 21 W



Paper No. : 5.9 & 13.1

Haswell: A Family of IA 22nm Processors

C. Honl, D. Sutherland, F. Hamzaoglu, N. Kurd, M. Chowdhury, E. Burton, T.P. Thomas, C. Mozak, B. Boswell, M. Lal, A. Deval, J. Douglas, M. Elassal, A. Nalamalpu, T.M. Wilson, M. Merten, S. Chennupaty, W. Gomes, R. Kumar, U. Arslan, N. Bisnik, S. Ghosh, N. Lindert, M. Meterelliyoz, R.B. Osborne, J. Park, S. Tomishima, Y. Wang, K. Zhang

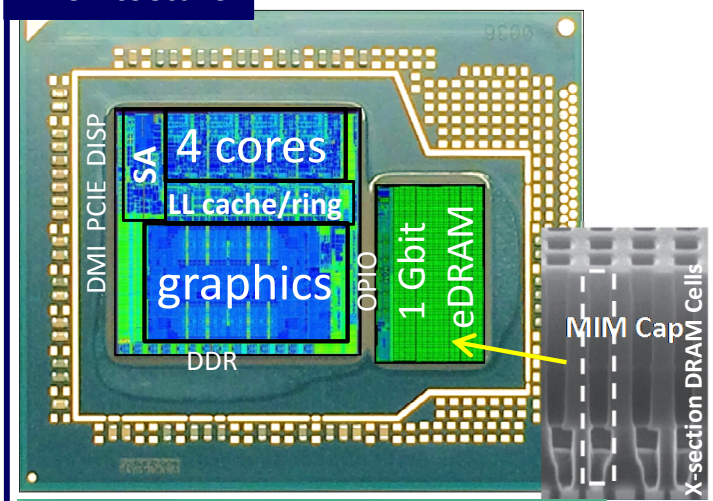
Intel, Hillsboro, OR

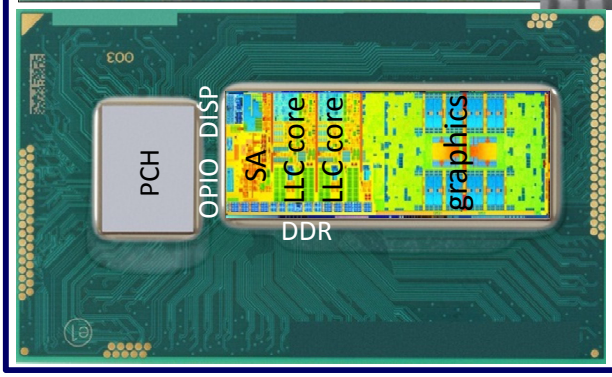
Motivation

High Level Goals for 'Haswell', 4th generation Intel® Core™ processor

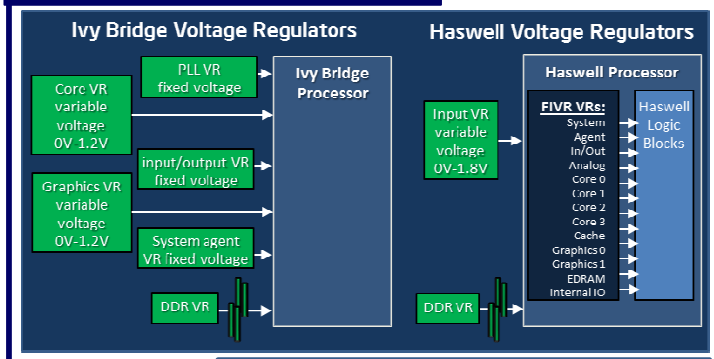
- **Span full product range, targeting best-in-class from fan-less Ultrabooks™ to high-end desktops and servers**
- **Enable 50% or more improvement in battery life**
  - Reduce standby power by 95%, by adding deeper sleep states with fast entry-exit times
  - Improve active power-performance, with wider architectures, at lower voltages, on lower-impedance fully integrated voltage regulators (FIVR)
- **Enable sleeker form factors and lower cost**
  - Integrate up to 13 voltage regulators (FIVR)
  - Integrate PCH & eDRAM with on-package I/O (OPIO)
  - Replace entry/mid-level discrete graphics with improved integrated graphics
- **Improve performance**
  - Double the vector throughput of integer and floating point operations
  - Double the graphics hardware and 4x bandwidth by eDRAM (102GB/s OPIO at 1.22pJ/b)
  - Leverage FIVR's low impedance for performance

Architecture

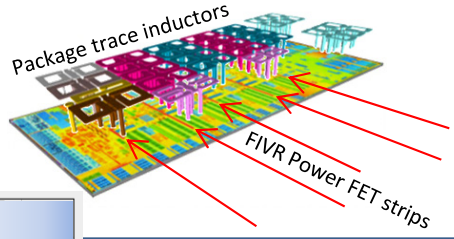


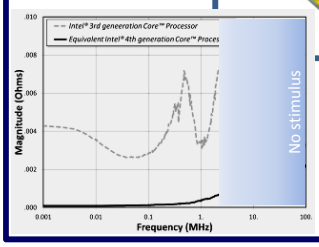


System Implementation



FIVR – Fully Integrated VRs





FIVR – 7.5mΩ → 0.5mΩ AC impedance;
→245mV droop reduction w/ 35A step

Verification

C7 → burst → C7 | 1080p video streaming

eDRAM OFF: 23 frames/s | eDRAM ON: 46 frames/s

Package State	Actions taken in various Package States	Haswell CPU Power (Watts)	Ivy Bridge CPU Power (Watts)
C0	Cores, Graphics actively executing	15 W (TDP)	17 W (TDP)
C6	Core's and Graphics powered off. DDR in self refresh. Most PLL's off.	0.9	2.3
C7	System agent and DDR IO power gated. CPU critical arrays powered by Sustain Rail.	0.85	2.2
C8	Display and IO rails off. Last level cache flushed. System Agent gated. Vin = 1.2V.	0.077	N/A
C9	Vin is lowered to 0V.	0.018	N/A
C10	Vin VR turned off, other controllers in low power modes. Platform power target of 100mW or better.		N/A

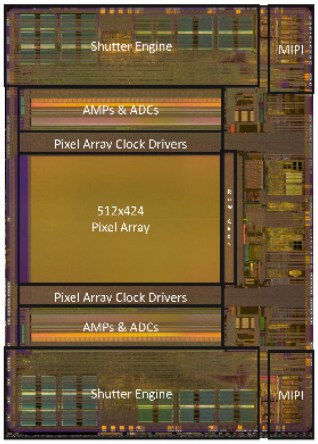
A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC

Cyrus S Bamji, et al.
Microsoft Corp., Mountain View, CA

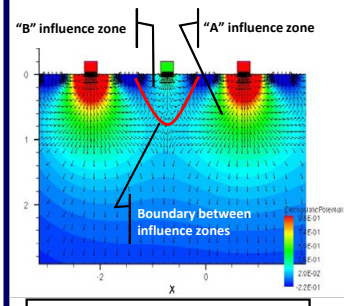
Objective

This demo presents the 3D depth camera in Kinect for XBOX one. This Camera contains a 512×424 CMOS 3D Time-of-Flight (ToF) Image Sensor running with multi-shutter, multi frequency and multi-phase operation

This ToF technology provides an accurate high resolution, low motion blur, wide field of view (FoV), high dynamic range depth image as well as an ambient light invariant brightness image (active IR) that meets the highest quality requirements for 3D motion detection.



Quantum Efficiency Modulation (QEM)



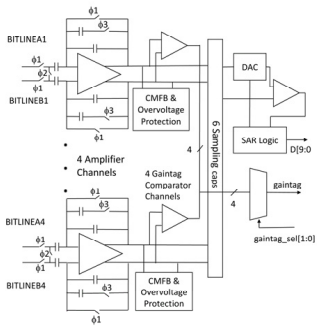
- A and B alternate high/low
- Light synchronized with A/B clock
- When A is high most electrons captured by A
- When B is high most electrons captured by B
- Charges never transferred from A to B

Charge Transfer (CCD like) | **QEM (This work)**

Charges collected but not assigned to gate A/B → Collect → Charges collected and simultaneously assigned to gate A/B

Charges must be stored in n+ for assignment to be complete. → Assign → Advantageously storage to n+ collection node can happen at leisure

→ Store



The analog outputs from pixels drive a 10-bit 8MS/s space efficient 0.027mm2;successive-approximation ADC. Total of 256 ADCs on the chip produce over 2GS/s thus converting a full chip image capture in approximately 100µs. Digitized output from the ADCs flows into the Shutter Engine which choreographs CDS, multi-shutter and multi-gain.

Features

Active IR imaging

- Depth and active IR images are produced by combining multiple images that are independent of ambient light.

High Resolution

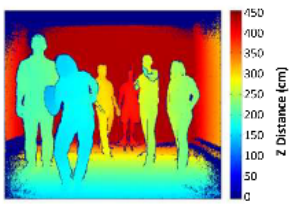
- Fine depth details present in the data including wrinkles in the clothes, buttons.

Large Field of View (FOV)

- Camera can detect up to 6 persons at 3m distance.

Low Motion Blur

- Camera can accurately handle fast moving objects.



Performance

High Modulation Contrast

- QEM Method works efficiently at high modulation frequency (10-130Mhz, MC=67%@50Mhz) and has low sensitivity to CMOS defects.

High Dynamic Range

- Each Pixel independently selects optimal Shutter time or Amplifier Gain

Low jitter and long operating range

- Multi frequency operation allows high operating frequency which is disambiguated using multiple frequencies.

High Accuracy

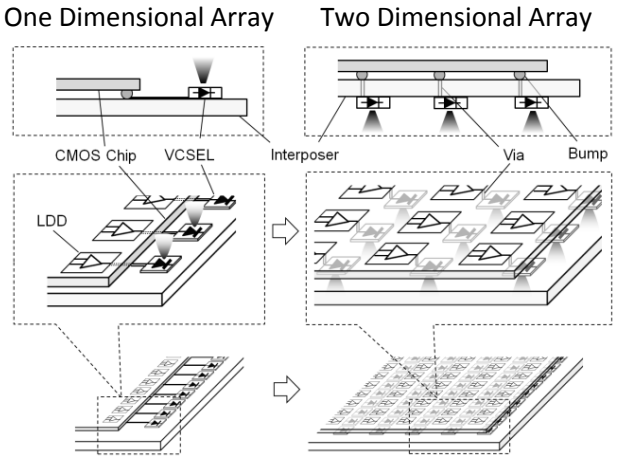
- Multi Capture method cancels harmonics and makes operation insensitive to temperature and component variations

Process Technology	TSMC 0.13 1P5M
Pixel Pitch	10u*10u
Pixel Array	512*424Pixels
Chip size	8.2mm*14.2mm
System Dynamic Range	> 2500 = 68db
Modulation Contrast	68% @ 860nm @50Mhz
Modulation Frequency	10-130Mhz
Average Modulation Frequency	80Mhz
FOV	70 (H) X 60 (V) degrees
Depth Uncertainty	< 0.5% of range
Distance Range	0.8-4.2m
Operating Wavelength	860nm
Frame Rate	max 60fps (typical 30fps)
ADC	2GS/s
Effective Fill Factor	60%
Reflectivity	15%-95%
Chip Power	2.1W
Responsivity @ 860nm	0.144 A/W
Readout Noise	320 uV differential
F#	1.07
ADC Resolution	10

A 12 × 5 Two-Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS

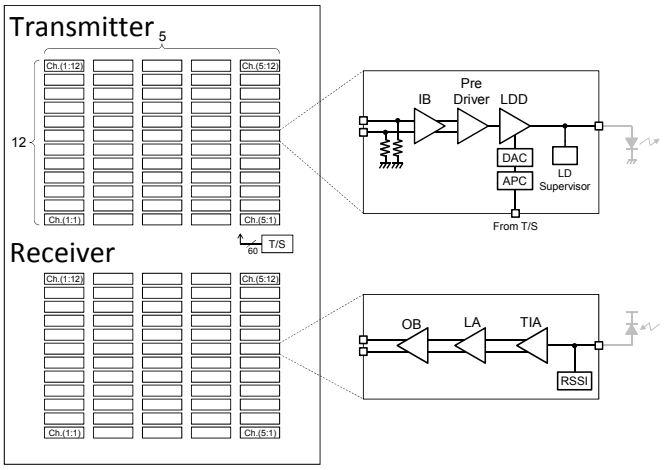
Hiroshi Morita, Koki Uchino, Eiji Otani, Hiizu Ohtorii, Takeshi Ogura, Kazunao Oniki, Shuichi Oka, Shusaku Yanagawa, Hideyuki Suzuki
Sony, Tokyo, Japan

Motivation



- High performance systems such as servers require high bandwidth interconnections
- Two dimensional optical I/O array relaxes the bandwidth limitation

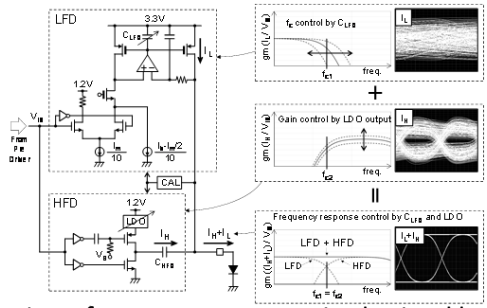
Architecture



- The transmitter and the receiver each have 60 channels organized in a 12 × 5 matrix
- The optical devices also have the same pitch as LDDs and TIAs
- The equalizer in IB compensates for high frequency loss with a range of 0dB to 9dB at 6GHz
- The LA amplifies the signal to a full-swing level, and the OB drives the 50Ω TL

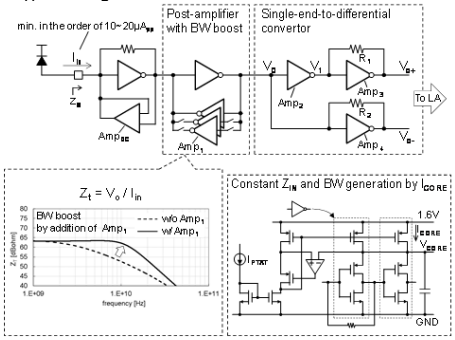
System Implementation

TX



- A flat gain vs frequency response is obtained by summing I_H and I_L

RX

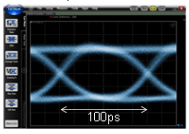


- All of the buffers are comprised of CMOS Inverter units
- High frequency boost is applied via the post-amplifier with positive feedback

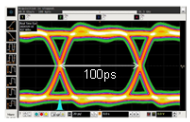
Verification

TX and RX eye diagram

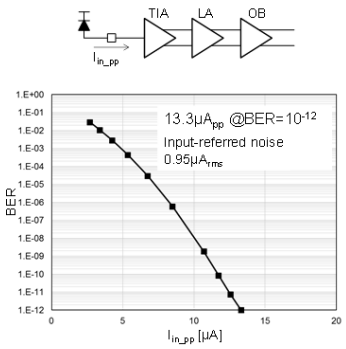
Optical eye diagram at LDD output



Electrical eye diagram at receiver after de-embedding board transmission line



RX sensitivity



LDD		
Process technology		CMOS 65nm
LDD type		LFD + HFD
Total data rate (Gb/s)		600Gb/s
Supply voltage of LDD		3.3V, 1.2V
Power dissipation of LDD at Ib=7mA, Im=8mA	w/o VCSEL	2.17mW/Gb/s
Area		510μm x 250μm

TIA		
Process technology		CMOS 65nm
TIA type		CMOS Inverter
Total data rate		600Gb/s
Supply voltage of TIA		1.6V
Power dissipation of TIA		0.96mW/Gb/s
Sensitivity at BER<10^{-12}	Input-referred noise	0.95μA$_{rms}$
Area		170μm x 25μm

- The power consumption of the LDD is 21.7mW/ch not including the power dissipation of VCSEL at 2V
- The TIA power consumption is 9.6mW/ch

A Self-Calibrating NFC SoC with a Triple-Mode Reconfigurable PLL and a Single-Path PICC-PCD Receiver in 0.11µm CMOS

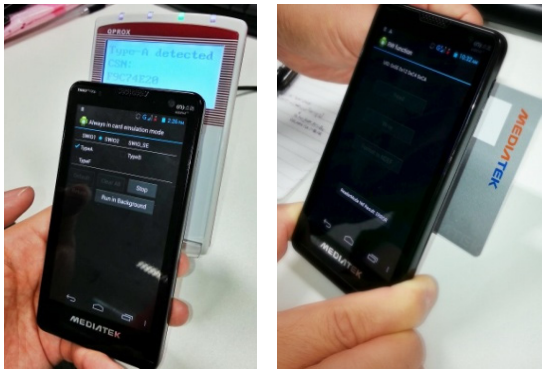
W. L. Lien[1], T. Y. Choke[1], Y. C. Tan[1], M. Kong[1], E. C. Low[1], D. P. Li[1], L. Jin[1], H. Zhang[1], C. H. Leow[1], S. L. Chew[1], U. Dasgupta[1], C. H. Yong[1], T. B. Gao[1], G. T. Ong[1], W. G. Tan[1], W. Shu[1], C. L. Heng[1], O. Shana'A[1,2].

[1]MediaTek, Singapore, Singapore; [2]MediaTek, San Jose, CA

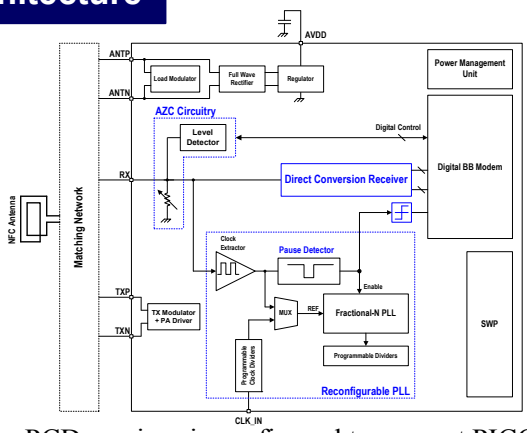
Motivation

To demonstrate the feasibility of using the PCD receiver with reconfigurable PLL to support PICC operations (D1), including joint data type detection (D2), and to leverage on it to significantly reduce the PCD low card power polling mode current (D3).

D1 Successful PICC operation with PCD receiver.
D2 PICC receiver is able to perform joint data type detection.
D3 Significantly reduced low power card polling current consumption.



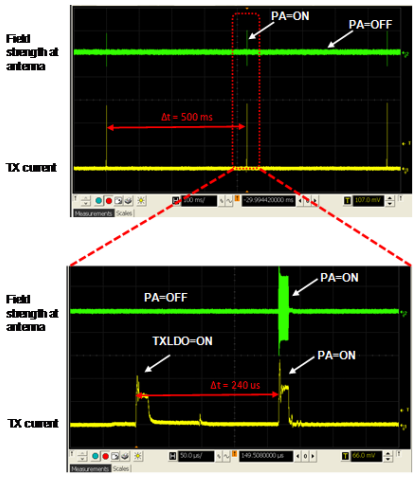
Architecture



1. PCD receiver is configured to support PICC operation by adding an AZC circuit. Pause detector with 1-bit ADC acts as analog PICC demodulator for NFC-A data. This helps improve joint-detection performance.
2. Reconfigurable PLL acts as a frequency synthesizer in PCD mode, and as a clock recovery module in PICC mode.
3. PCD receiver configured into low-IF mode to detect the change in TX power level during low-power card polling mode.

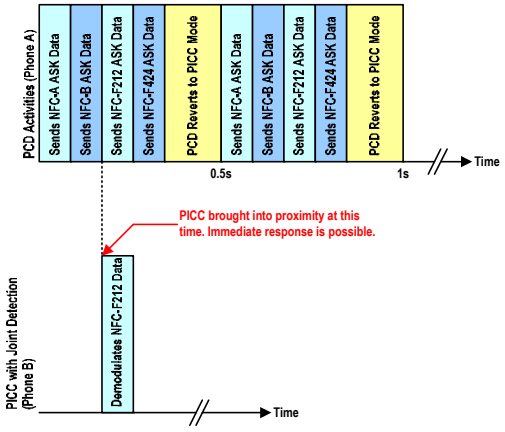
System Implementation

D1 Details described in Paper 9.1.
D2 Joint detection: Digital modem receives signals from single receiver and 1-bit ADC for immediate data type detection and demodulation.
D3 Low power (LP) polling scheme: Highly sensitive RX is re-configured to detect a change in TX power, shortening the detection time and LP polling current.



Verification

D1 Phone configured to PICC mode communicates successfully with various commercial readers.
D2 Phone A, configured to PCD mode, sends a very slow polling sequence. Phone B, configured to joint-detection PICC mode, responds immediately upon the first reception of a poll.



D3 Phone is configured into low power polling mode. Ammeter connected to NFC chip supply illustrates the low current consumption in this mode.

A 0.33nJ/b IEEE802.15.6/Proprietary-MICS/ISM-Band Transceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications

Maja Vidojkovic[1], Xiongchuan Huang[1], Xiaoyan Wang[1], Cui Zhou[1], Ao Ba[1], Maarten Lont[1], Yao-Hong Liu[1], Pieter Harpe[2], Ming Ding[1], Ben Busze[1], Nauman Kiyani[1], Kouichi Kanda[3], Shoichi Masui[3], Kathleen Philips[1], Harmke de Groot[1]

[1]Holst Centre/imec, Eindhoven, The Netherlands

[2]Eindhoven University of Technology, Eindhoven, The Netherlands

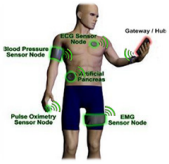
[3]Fujitsu Laboratories, Kawasaki, Japan

Motivation

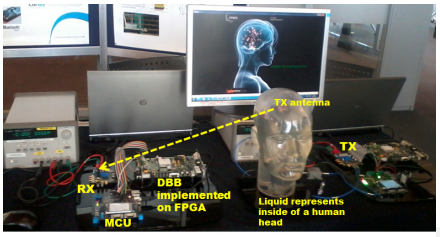
ULP 400MHz Radio for WBAN Applications:

- ✓ Highly reconfigurable for various modes:
  - ✓ IEEE 802.15.6-WBAN standard compliant
  - ✓ 4.5Mb/s high speed proprietary mode for high date rate streaming (e.g. EEG)
  - ✓ 11kb/s low speed proprietary control mode
  - ✓ Programmable for node and hub
- ✓ State-of-the-art performance

IEEE 802.15.6-NB (WBAN)

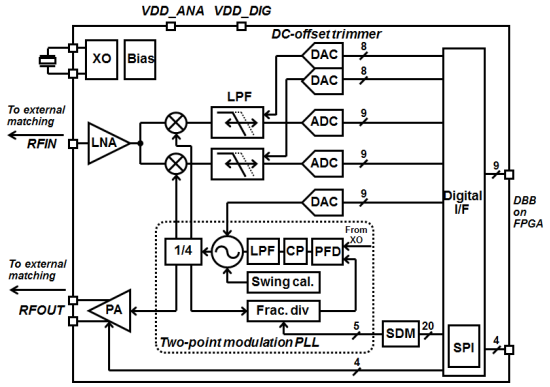


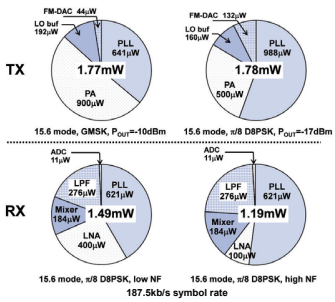
High data rate streaming EEG



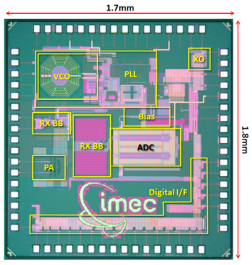
Demonstration setup of the wireless link

Transceiver Architecture





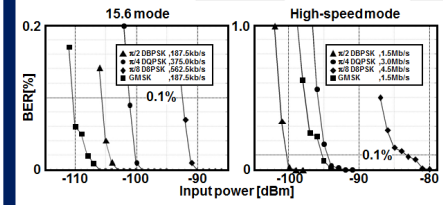
Power breakdown



Chip Photo (TSMC 40nm)

Performance

Receiver performance



Sensitivity

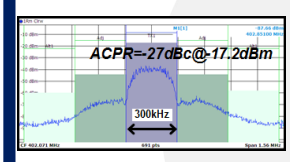
ACR in 15.6 mode (@0.01% BER)

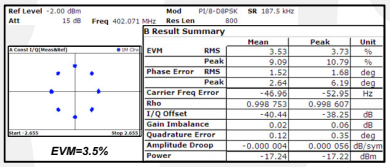
Modulation	Data rate [kb/s]	ACR [dB] Meas.	ACR [dB] Spec.
π/2 DBPSK	187.5	15	14
π/4 DQPSK	375	14	10
π/8 D8PSK	562.5	8	5

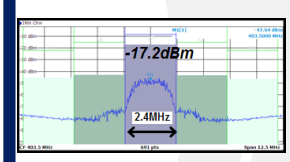
All the data rates without BCH code

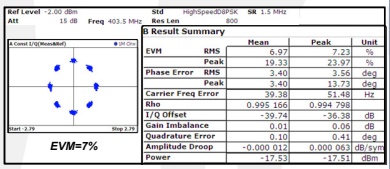
Adjacent channel rejection

Transmitter modulation performance









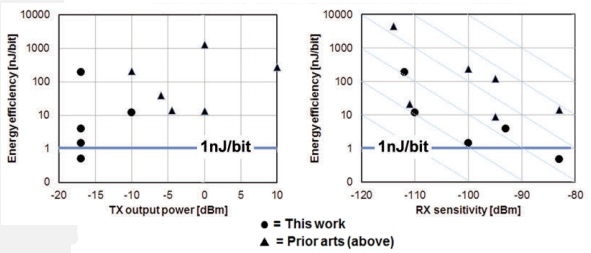
Adj. channel leakage

Modulation accuracy

400MHz Radio Benchmark

			ADF7021-V Analog Devices	nRF9E5 Nordic	CC1101 TI	BioCAS Dec.'06 pp.188-161	ISSCC'05 pp.288-289	ESSCIRC '09 (*3) pp.232-235	This work				
Standard			-	-	-	-	-	-	IEEE 802.15.6		-	-	-
Modulation			2/3/4-FSK MSK	GFSK	2/4-FSK GFSK, MSK, ASK, OOK	2/4/8-FSK	FSK OOK	GFSK π/4-DQPSK	GMSK	π/8 D8PSK	π/2 DBPSK	π/2 DBPSK	π/8 D8PSK
Frequency band		MHz	431-475	433	387-464	402-405 432-434	433	401-406	402-405 420-450				
Data rate, min/max		kb/s	0.05 / 24	100	0.6 / 600	200 / 800	2 / 100	- / 400	10 / 4500				
TX output power, min/max		dBm	-16 / +13	-10 / 10	-30 / +10	-17 / -4.5	- / 10.5	- / 0	-20 / -5				
Technology			-	-	-	0.18μm	0.18μm	0.13μm	40nm				
Supply voltage, min/max		V	2.3 / 3.6	1.9 / 3.6	1.8 / 3.6	2.1 / 3.5	1.0 / 1.6	1.2 / -	1.0 / -				
TX power consumption	Power	mW	31.74	20.9	23.58	11.55	27.6	5.4	2.27(*2)	2.28 (*2)			
	@P_{OUT}	dBm	0	-10	-6	-4.5	10	0	-10	-17			
RX power consumption	Power	mW	42.09	23.75	30.78	11.55	2.1	3.6	2.19 (*2)				
	@sensitivity	dBm	-114	-100	-95	-83 (*1)	-111	-95	-110	-93	-112(*4)	-100	-83
	@data rate	kb/s	9.6	100	250	800	25	400	187.5	562.5	11.7	1500	4500

(*1) Sensitivity in dBm was calculated with 90uV and 1600ohm given in the paper.
(*2) Simulated DBB power of 0.5mW(TX) and 0.7mW(RX) were added to the measured analog front-end
(*3) This IC does not have digital base-band on the same die of the analog front-end.
(*4) 6dB improvement from spreading factor increase from 1 to 16 is taken into account



The most energy-efficient 400MHz radio for medical applications!

Paper No. : 10.7

A 105 GOPS 36mm2 heterogeneous SDR MPSoC with energy-aware dynamic scheduling and iterative detection-decoding for 4G in 65nm CMOS

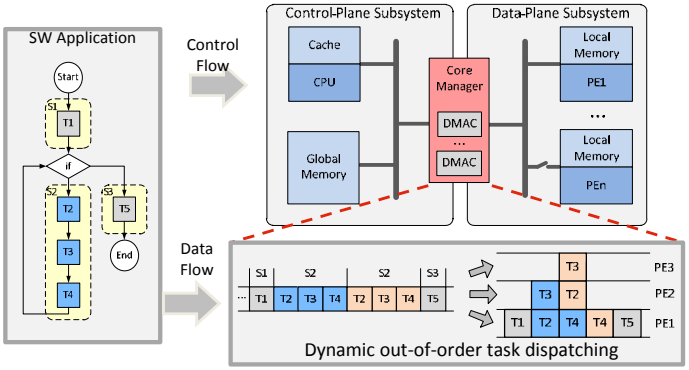
Benedikt Noethen, Oliver Arnold, Esther P. Adeva, Tobias Seifert, Erik Fischer, Steffen Kunze, Emil Matus, Gerhard Fettweis, Holger Eisenreich, Georg Ellguth, Stephan Hartmann, Sebastian Höppner, Stefan Schiefer, Jens-Uwe Schlüßler, Stefan Scholze, Dennis Walter, René Schüffny

Motivation

Challenges:

- Energy-efficient MPSoC solution needed to meet power constraints (e.g. femto basestations)
- Set of applications to be executed concurrrently
- Map tasks efficiently to heterogenous set of processing elements (PEs)

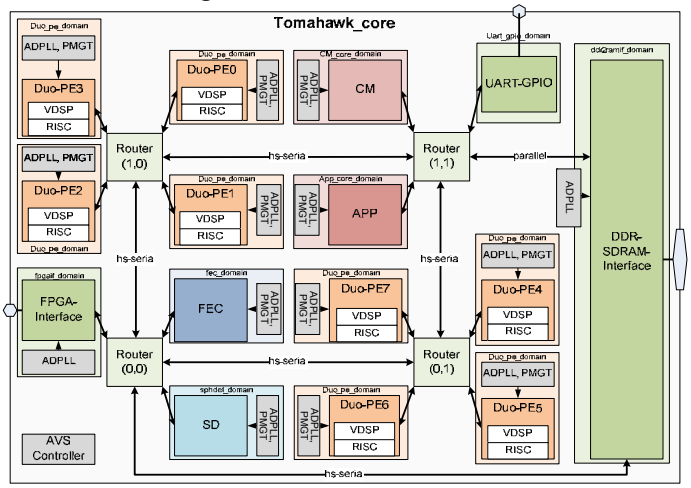
Approach: CoreManager (CM) Concept



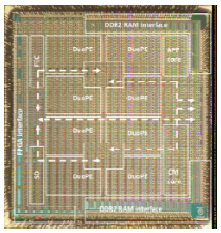
- Application-specific instruction set (up to 200x faster and 150x more energy efficient compared to RISC-based CoreManager implementation)
- Energy-managment at runtime (System- and PE-level)
- Flexible dynamic task-scheduling (deadline or priority based)
- Dynamic PE and local memory allocation, including explicit data transfer management
- Data dependency checking at runtime

Architecture

Overall Block Diagram:



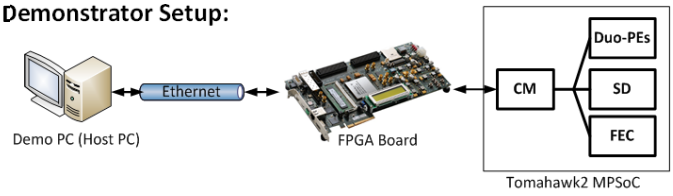
Chip Implementation/Facts



- TSMC 65 LP CMOS
- Area: 6mm x 6mm
- Pads: 465
- Gates: 10,2 Mio.
- SRAM: 750 kByte
- Fine granular DVFS/AVFS on PE Level
- Voltage: adaptable between 0.7-1.3V
- Frequency range: 86 – 500 MHz

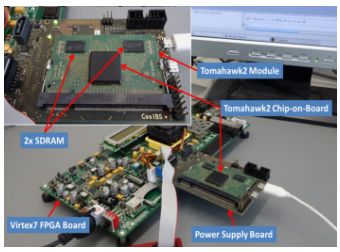
System Implementation

Demonstrator Setup:



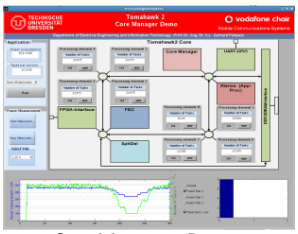
Tomahawk2 Demonstrations:

- Iterative MIMO detection-decoding: power consumption and communications performance
- Dynamic task-scheduling: performance and power scalability

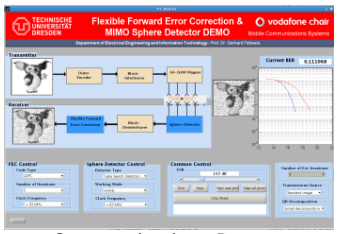


<Test Board System Setup>

Host-PC Visualization:



<CoreManager Demo>



<Communications Demo>

Verification

		Area [mm2] *total*	Area [mm2] *mem*	Mem size [bit]	f_{max} [MHz] @VDD =1.2 V	Throughput @f_{max}	P [mW] @f_{max}, VDD=1.2 V
APP		0.582	0.245	274432	445	890 MOPS	49.7
CM		1.360	0.870	786432	445	1.1 MTasks/s	74.6
Duo -PE[a]	Xtensa	1.357	0.800	532480	445	890 MOPS	61.5
	VDSP				500	10 GOPS	98.1
SD		0.522	0.260	292864	445	396 Mb/s	87.0
FEC		1.154	0.618	479232	500	155 Mb/s	360.0
FPGA-IF		0.602	-	-	500	10 Gb/s	-
DDR-IF		4.552	-	-	400	12.8 Gb/s	-
NoC		3.417	-	-	500	80 Gb/s[b]	32.0[c]

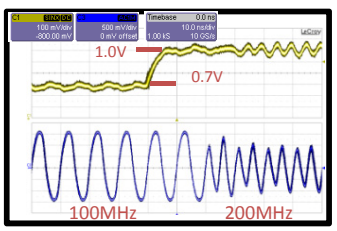
[a] Per instance. [b] Per link, max throughput. [c] Averaged over several test cases, NoC not fully utilized

<Component Overview of the MPSoC>

	Technology [nm]	NoC Throughput [Gbit/s/link]	Peak Performance [GOPS]	Power Consumption [mW]
This	65	80	105	480
[1]	65	17	37	477
[2]	130	5.47	40	1200

<Performance Comparison>

[1] F. Clermidy, et al., "A 477mW NoC-based digital baseband for MIMO 4G SDR," ISSCC Dig. Tech. Papers, pp. 278-279, 2010.
[2] D. Ilitzky, et al., "Architecture of the Scalable Communications Core's Network on Chip," IEEE Micro, vol. 27, no. 5, pp. 62-74, 2007.



<Ultra fast DVFS>

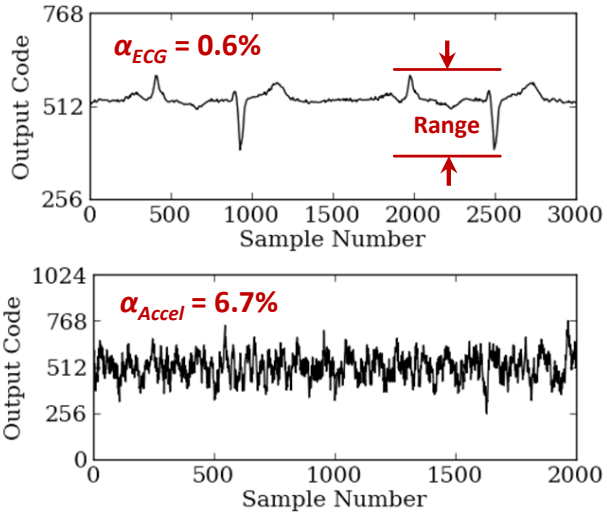
Paper No. : 11.3

A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation

Frank M. Yaul and Anantha P. Chandrakasan
Massachusetts Institute of Technology

Motivation

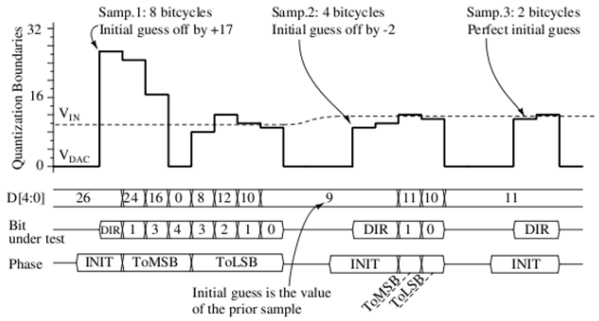
- On average, what fraction of its full range does the signal jump from sample to sample?
- Signal activity: $\alpha = \frac{\langle \Delta code \rangle}{Range}$

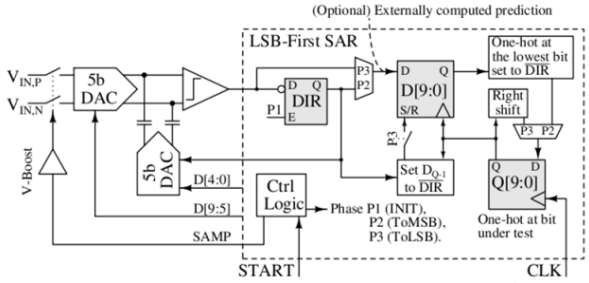


Exploit low activity using altered successive approximation algorithm

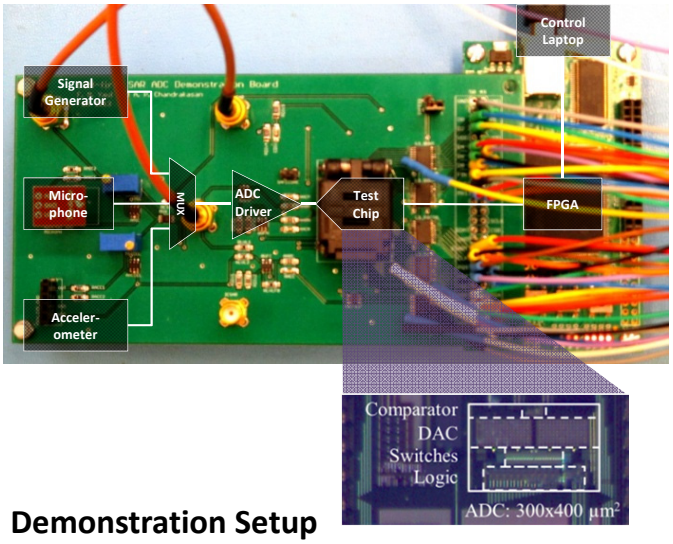
Architecture

Key Idea: Start search with an initial guess (previous sample). Use fewer bitcycles when initial guess is close to final output code.





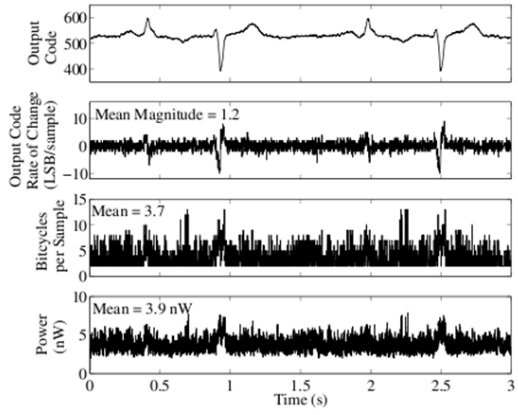
System Implementation



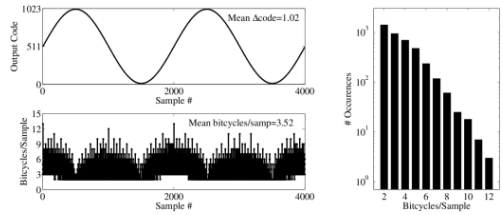
Demonstration Setup

- Sensor outputs and analog signal chain drive the ADC
- Observe ADC performance for different types of signals

Verification



ADC response to ECG input at 0.5V and 1kS/s.
Averages 3.7 bitcycles for 10b conversions.



Most code transitions shown to use few bitcycles.

Paper No. : 12.1

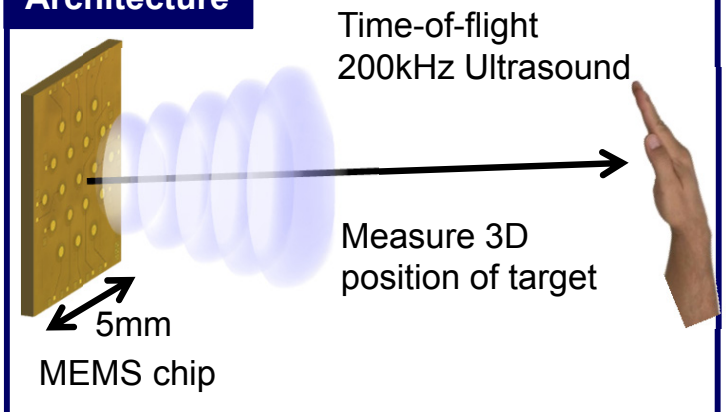
3D Ultrasonic Gesture Recognition

Richard J. Przybyla[1], Hao-Yen Tang[1], Stefon E. Shelton[2], David A. Horsley[2], Bernhard E. Boser[1]
University of California, [1]Berkeley, CA and [2]Davis, CA

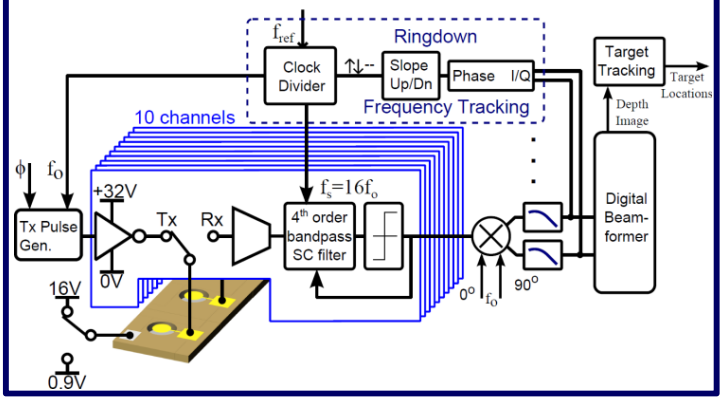
Motivation

Gesture interaction is a natural way to control your devices. Unfortunately, **optical 3D rangefinders are too large, sunlight sensitive, and power hungry** to be incorporated in an energy-constrained environment such as a mobile device. **Gesture recognition using sound** is an attractive candidate to overcome these difficulties.

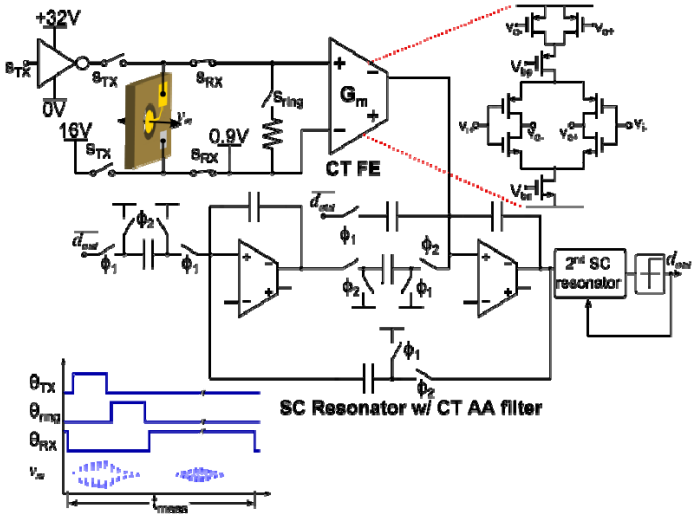
Architecture



10 channel TX/RX CMOS ASIC

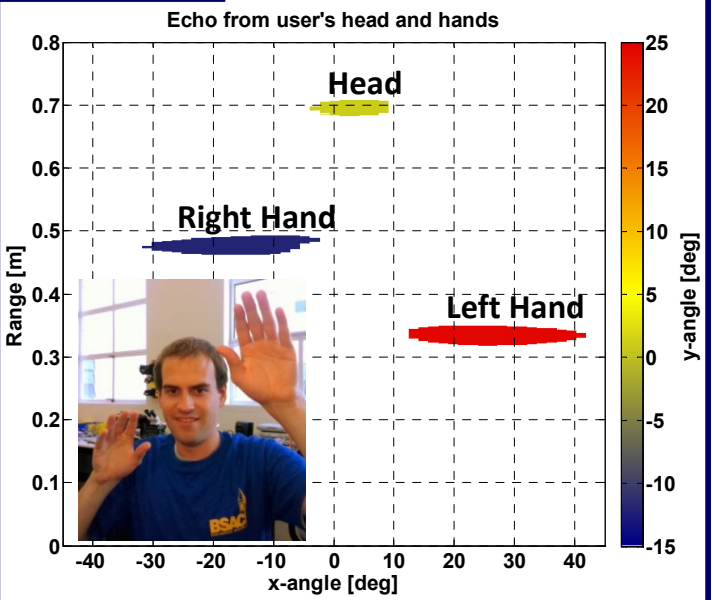


System Implementation



The system transmits a short pulse of ultrasound into the environment, and then listens for echoes from objects within 1m. The system automatically tunes to the resonant frequency of the MEMS ultrasound transducers, which each work as a transmitter and receiver.

Verification



This measured data shows the echo from a user's hands and head. The color encodes the vertical angle. **System power consumption is 400μW at 30 frames per second, or 14μJ/measurement.**

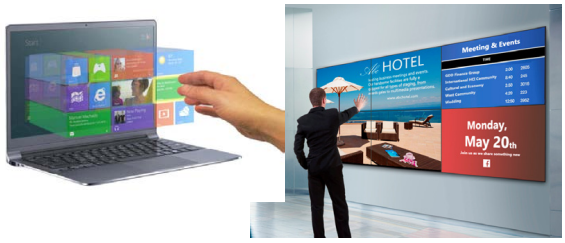
3D Gesture Sensing System for Interactive Displays based on Extended-range Capacitive Sensing

Paper No. : 12.2

Yingzhe Hu, Liechao Huang, Warren Rieutort-Louis, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma
Princeton University, Princeton, NJ

Motivation

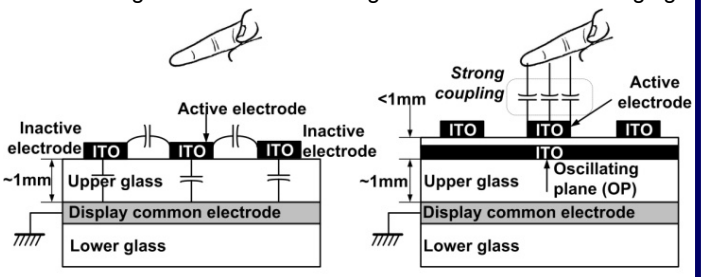
3D gesture sensing can substantially enrich user experiences



Capacitive sensing

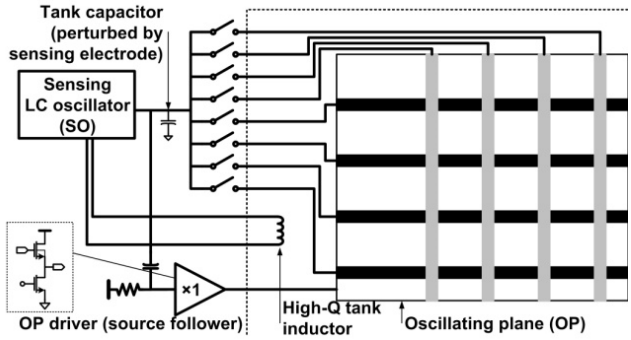
Advantages:
- low-cost ITO array integration for large display
- low-power readout (compared to video)
- no sight line needed (compared to video)

Disadvantages:
- short 3D sensing distance due to field fringing



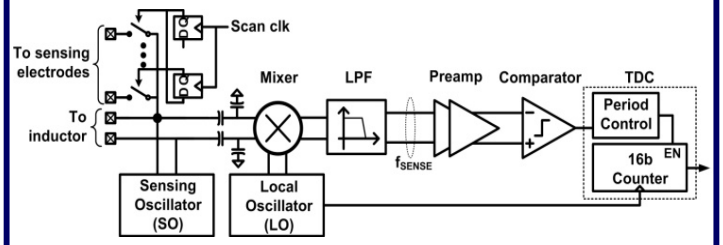
Solution:
Oscillating plane directs field from sensing electrode to greatly mitigate fringing at long distances

Architecture

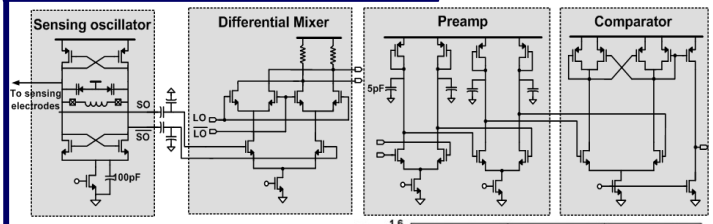


- **Capacitance sensing via high-Q oscillator enables increased sensitivity for greater distances**
- **Reduced number of electrodes (4x4) can be used for high-resolution sensing over large area**

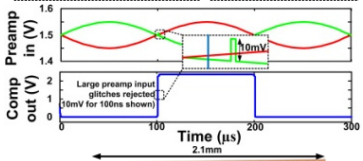
Frequency modulation readout via low-noise oscillators & TDC



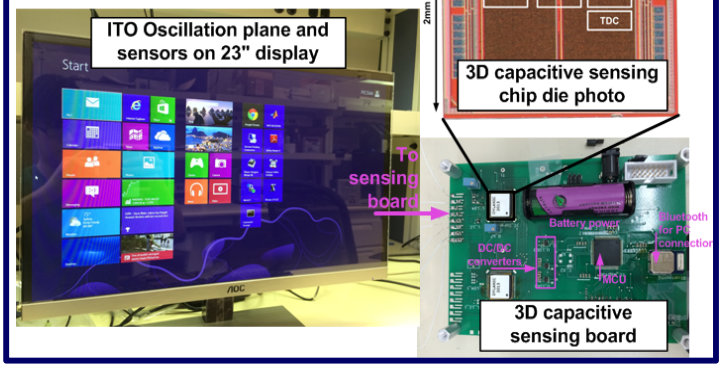
System Implementation



- High-Q oscillators reduce readout phase noise with low power consumption
- Preamp implements noise filtering with a cutoff frequency of 200kHz

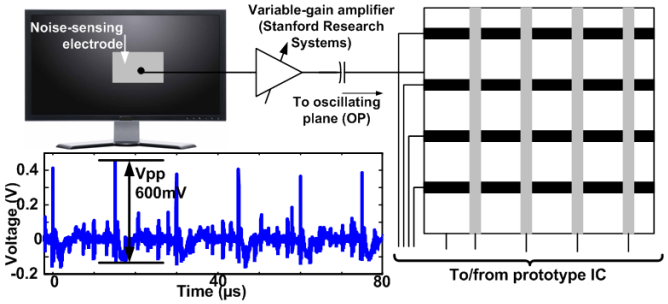


- **System demo implementation:**

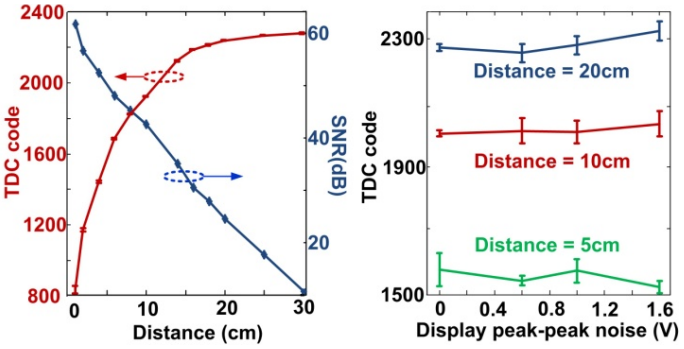


Verification

Testing setup:



Measurements:



Gesture recognition with distance larger than 20cm is achieved on 23" a display

Paper No. : 12.3

A 240Hz-Reporting-Rate 143 × 81 Mutual-Capacitance Touch-Sensing Analog Front-End IC with 37dB SNR for 1mm-Diameter Stylus

Mutsumi Hamaguchi[1], Akira Nagao[2], Masayuki Miyamoto[2]
[1]Sharp, Fukuyama, Japan, [2]Sharp, Tenri, Japan

Motivation

Realization of mutual capacitance touch sensing systems with

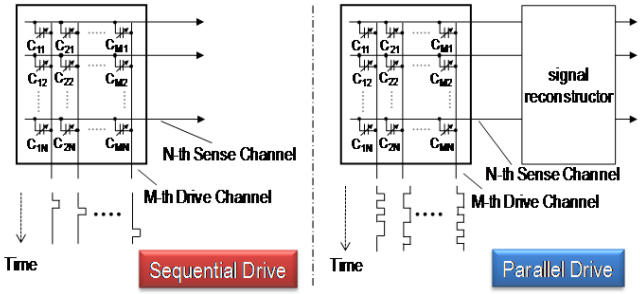
(1) Unified touch UI for all size of displays from 4-inch up to 100-inch,

(2) Fine pen handwriting without additional pen digitizer,

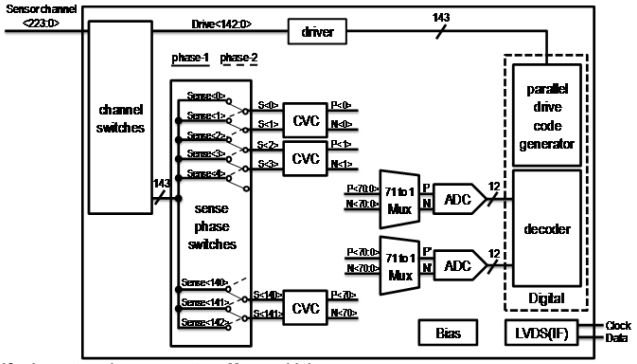
(3) Strong immunity against LCD noise.

Architecture

(1) Channels are driven in parallel. Appropriately designed parallel drive sequences enhance the SNR by √M times compared to that of the sequential drive.



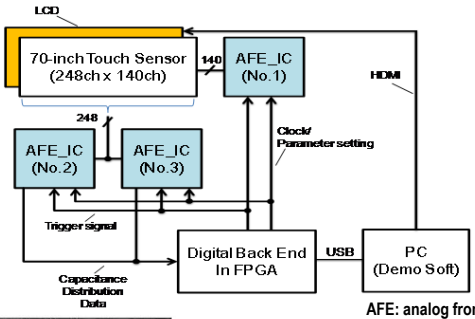
(2) A fully differential sensing scheme cancels the strong LCD noise commonly injected into adjacent channels. In phase-1 (the first differential signal sensing), the (2i+1)-th and the 2i-th sense channel are connected to the i-th CVC's Inputs, while in phase-2 (the second differential signal sensing), the (2i+2)-th and the (2i+1)-th sense channel are connected to the i-th CVC's Inputs, where i=0, …, 70.



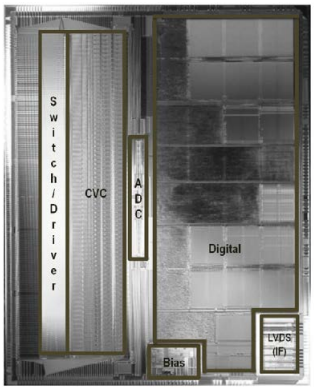
CVC: charge-to-voltage converter Mux: multiplexer
ADC: analog-to-digital converter LDVS: low-voltage differential signaling

System Implementation

A 32-inch and a 70-inch system are realized with the use of the AFE and a 7μm thickness copper mesh sensor technology. The 70-inch system is built up from three AFEs, a DBE implemented in an FPGA, 6.25mm channel pitch 248 × 140 metal mesh sensor laminated to a 1.9mm thickness cover glass, and mounted on a FHD LCD with 3.24mm air gap.



AFE: analog front-end



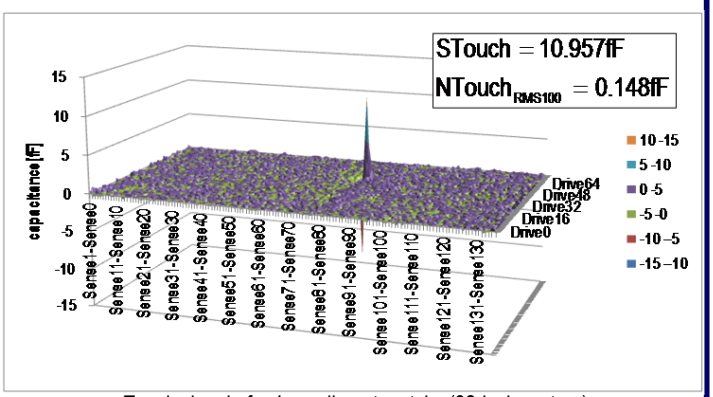
The die size is 7.55 × 9.43mm² including 0.2mm scribe line. It is assembled in an 18 × 18mm² ball grid array (BGA) package with 364 balls.

Verification

[3] J.-H. Yang, ISSCC 2013
[4] H. Shin, ISSCC2013

		[3]	[4]	This work			
Size[inch]		10.1	5	32		70	
Number of channels		27ch (Tx) x 43ch(Rx)	30ch(Tx) x 24ch(Rx)	78ch(Tx) x 138ch(Rx)		140ch(Tx) x 248ch(Rx)	
Mode		Undescribed	High SNR (CDMS DS-SC)	Slow	Normal	Slow	Normal
Reporting rate[Hz]		120	240	120	240	120	240
SNR[dB]	Finger	39	55	50.8	56.6	47.5	52.2
	Pen (1mmΦ)	Undescribed	35	31.6	37.4	31.5	37.7
Process		0.35μm CMOS	2P6M 0.18μm CMOS EEPROM	1P5M 0.18μm CMOS			
Power consumption	Total [mW]	18.7	52.8	214.7	559.9	562.8	1247.0
	Per node [uW/node]	16.1	73.3	19.9	52.0	16.2	35.9
Supply voltage		3.3V	3.3V	3.3V, 1.8V			
Die size		4mm x 4mm	4.06mm x 3.66mm	7.55mm x 9.43mm			

Specification and performance summary



Touch signal of a 1mm diameter stylus(32-inch system)

Paper No. : 12.4

A 1mm-Pitch 80x80-Channel 322Hz-Frame-Rate Touch Sensor with Two-Step Dual-Mode Capacitance Scan

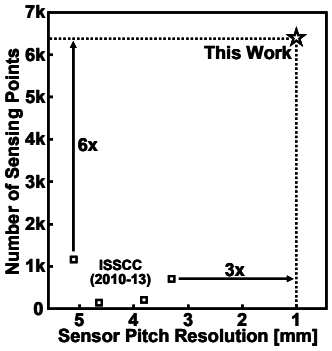
N. Miura[1], S. Dosho[2], S. Takaya[1], D. Fujimoto[1], T. Kiriyama[1], H. Tezuka[2], T. Miki[2], H. Yanagawa[2], M. Nagata[1]
[1]Kobe University, [2]Panasonic Corporation, Japan

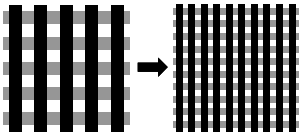
Motivation

►**High-resolution and large-area touch sensor for interactive and natural human interfaces**

Electronic Whiteboard

Interactive Digital Signage





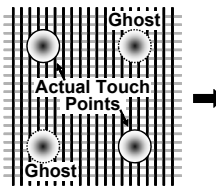
1.5x Frame Rate (322Hz) even for 6x Scan Points

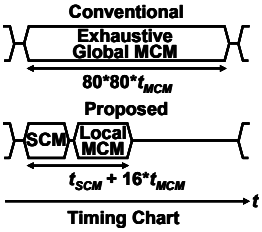
Keep SNR (41dB) even with 1/10 Size Electrode

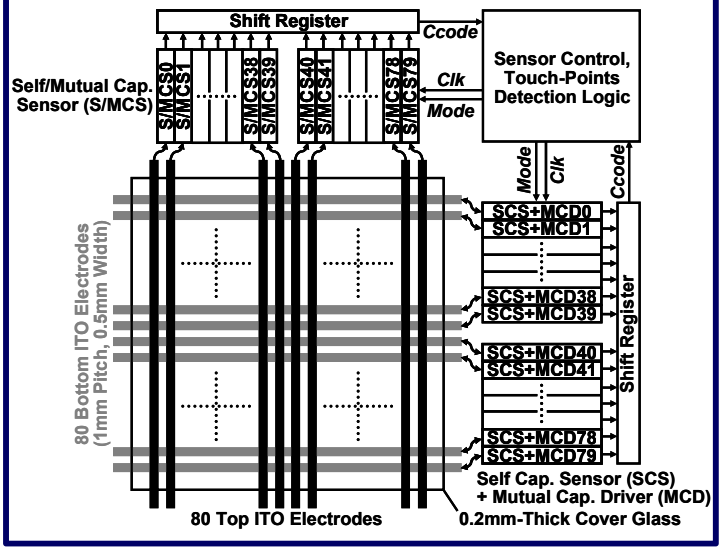
10x High-Speed and yet 10x Low-Energy-Consumption High-Resolution Touch Sensor with 1/4 Silicon Chip Area in 0.35µm CMOS

Architecture

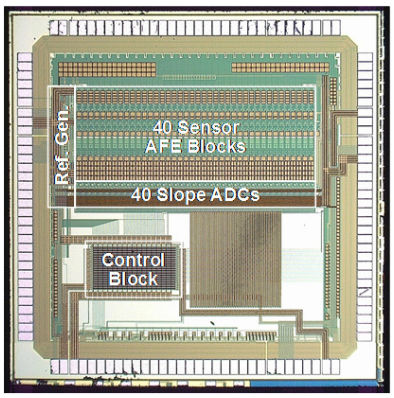
►**Two-Step Dual-Mode Capacitance Scan Scheme**

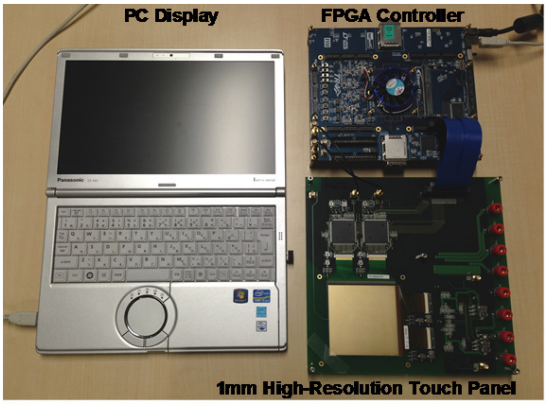




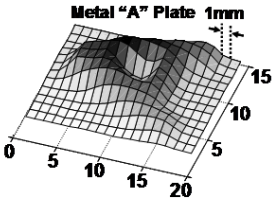


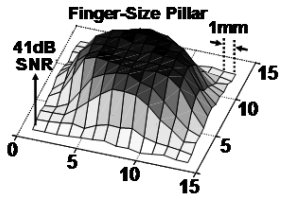
System Implementation





Verification





	J.-H. Yang, (ISSCC'13)	H. Shin, (ISSCC'13)	This Work
Capacitance Sensing Type	Mutual	Mutual	Self/Mutual Dual Mode
Channel Pitch	5mm	3mm	1mm (1/3)
Number of Channels	27x43	24x30	80x80 (5.5x)
Touch Panel Size	10.1"	5"	4.5"
Frame Rate Scan Points / Sec.	120Hz 0.14Mpoints/s	240Hz 0.17Mpoints/s	322Hz 2.06Mpoints/s
Power Consumption Energy / Channel	18.7mW 134nJ/ch	52.8mW 306nJ/ch	21.8mW 11nJ/ch (1/12)
Chip Layout Area Area / Channel	10.4mm² 896µm²/ch	14.9mm² 2069µm²/ch	13.7mm² 214µm²/ch (1/4)
SNR	39dB (Finger)	55dB (Finger) 35dB (1mm-ϕ)	41dB (Finger) 32dB (1mm-ϕ)
Process	0.35µm CMOS	0.18µm CMOS	0.35µm CMOS

Paper No. : 12.8

A BJT-based CMOS temperature sensor with a 3.6pJ°C² resolution FoM

A. Heidari[1,2,3], G. Wang[1,2], K.A.A. Makinwa[2] and G.C.M. Meijer[4,2,1]

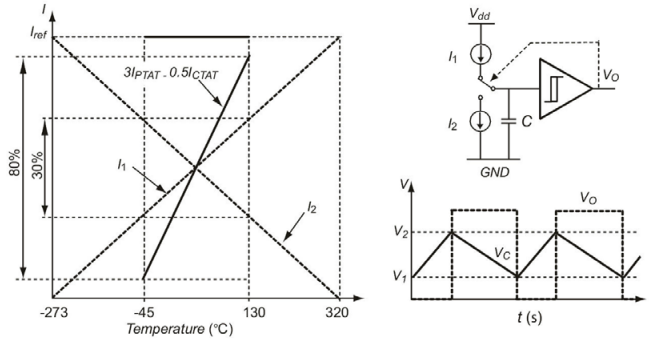
[1] Smartec, Breda, The Netherlands; [2] Delft University of Technology, Delft, The Netherlands;

[3] Guilan University, Rasht, Iran; [4] Sensart, Delft, The Netherlands

Motivation

Design targets

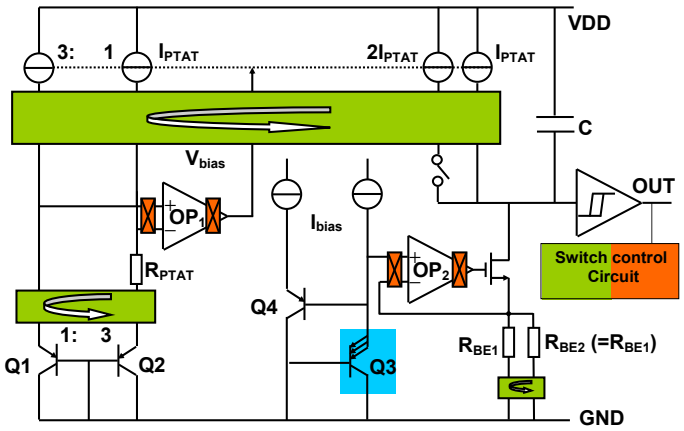
To implement a temperature sensor featured with ***low cost***, ***high accuracy***, ***high resolution***, ***fast response*** and ***high energy efficiency***



$$D = D_0 + ST$$

The duty cycle output can easily be interfaced to the digital as well as to the analog world

Architecture

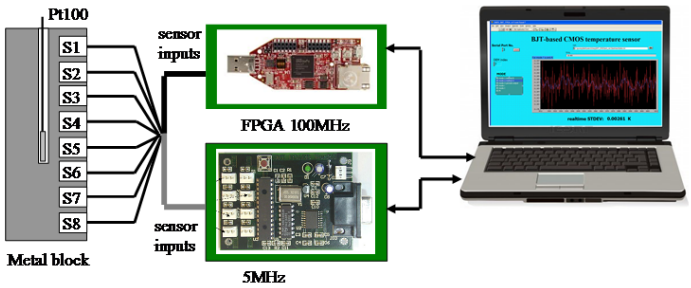


Errors are reduced by:

- DEM
- Chopping
- Trimming

Accurate results are obtained after averaging over a complete DEM cycle (8 periods)

System Implementation

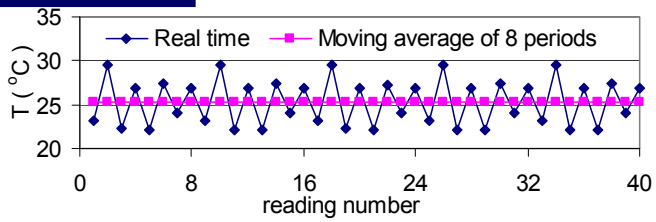


To test the sensor performances, the sensor output was read using

- A commercial FPGA board with a 100MHz counter to achieve low quantization noise.
- LabView software to display the result
- A Platinum resistor to measure the ambient temperature as reference

Low-cost microcontroller can be used too. However, with a low-frequency counter (5MHz), quantization noise dominates the measurement resolution

Verification



Typical sensor characteristics:

- Supply voltage range 2.9V to 5.5V
- Temperature range -45°C to 130°C
- Spreading of 15 samples less than 0.15°C
- Resolution FoM 3.6pJ°C² with
  - V_{dd} = 3.3V I_{sup} = 55uA
  - Resolution = 0.003°C for t_m = 2.2ms
  - One DEM cycle takes 2.2ms at room temperature

With a low-cost microcontroller (5MHz counter), system performance is

- Resolution = 0.02°C (moving average over 2.2ms)
  - Sensor noise is negligible
  - Quantization noise is dominant
- Resolution = 0.0032°C (moving average over 100ms)

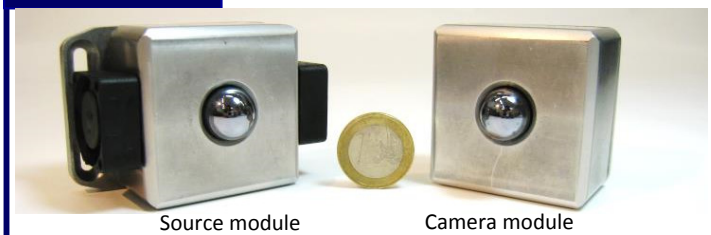
Paper No. : 14.5

A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13µm SiGe BiCMOS

U. Pfeiffer[1], Y. Zhao[1], J. Grzyb[1], R. Al Hadi[1], N. Sarmah[1], W. Förster[1], H. Rücker[2], B. Heinemann[2]

[1]University of Wuppertal, Wuppertal, Germany , [2]IHP, Frankfurt (Oder), Germany

Motivation



Source module Camera module

The 0.53THz source array demonstration module

Context and state of the art:

- The terahertz frequency range (300GHz–3THz) has many applications in imaging, sensing and high data rate communications
- Low-cost implementations of terahertz systems are challenging due to the limited cut-off frequency of devices in silicon technologies

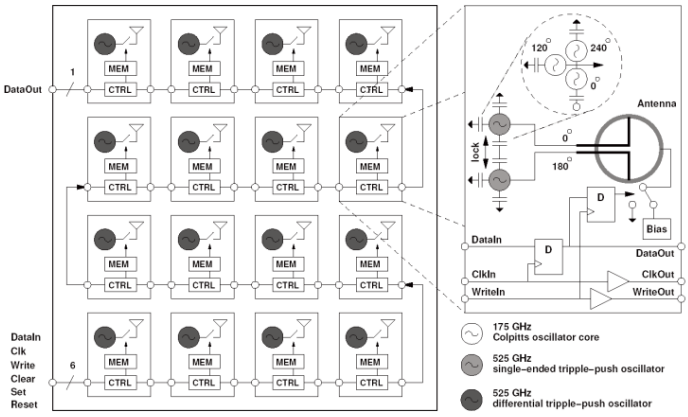
Technical highlights:

- This paper presents a reconfigurable 16-element radiator array at around 0.5THz in a 0.13µm BiCMOS process technology
- The radiation from each element is not coherent which makes the system simpler and more effective for terahertz imaging applications
- The radiated power from the array is 1mW which is enough for many imaging applications.

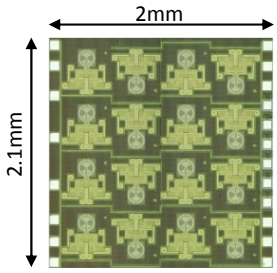
Application and economic impact:

- Portable terahertz sources can revolutionize the imaging and sensing applications
- There are many applications in security, bio-sensing, and imaging that would benefit from this work
- Low cost solutions allow rapid uptake of the technology

Architecture



Terahertz source array block diagram

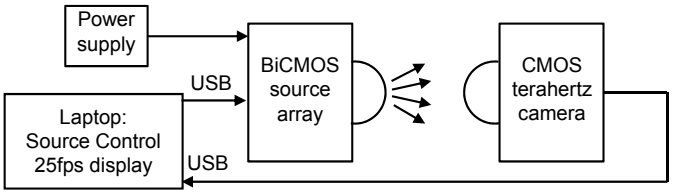


Chip Micrograph

Key features:

- 16 (4x4) pixels
- 0.13µm SiGe BiCMOS technology
- 1mW total output power at 0.53THz
- Average output power of 60µW/pixel
- Selectable patterns and lighting conditions
- 0.52-0.54GHz tuning range
- 40dBi Silicon lens
- EIRP of 25dBm

System Implementation



System Implementation Diagram

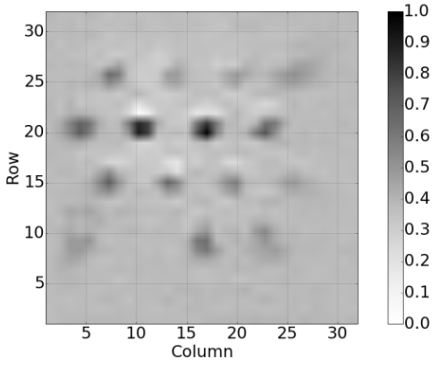
The terahertz source array is controlled via USB

- Programmable lighting condition in real-time
- Handheld terahertz device
- Silicon lens
- Clock generator
- Programmable logic control
- Regulated power-supplies
- Digital control interface
- Room temperature terahertz imaging demonstration

Setup

An arbitrary pattern is loaded into the BiCMOS terahertz source via USB. The source array illuminates a 1k-pixel CMOS terahertz camera module [1]. The real-time stream of the CMOS camera is displayed on the computer screen.

Verification



Still frame of the terahertz camera at 25 fps

Tech.	Freq. [GHz]	RP [dBm]	EIRP [dBm]	Pixel	BW [%]	Eff. [‰]	Area [mm^2]	Ref.
65nm bulk	260	0.5	15.7	8	9.5	1.4	2.3	[2]
65nm SOI	280	-7.1	9.4	16	3.2	-	7.3	[3]
65nm bulk	288	-4.1	14.2	1	0.7	1.4	0.29	[4]
45nm bulk	553	-36.5	-	1	-	3.40E-04	0.29	[5]
0.25µm SiGe	825	-29	-17	4	1.8	2.70E-04	3.22	[6]
0.13µm SiGe	**519-536**	**0**	**25**	**16**	**3.2**	**0.4**	**4.2**	**This Work**

[1] R. Al Hadi JSSC 2013, [2] R. Han JSSC 2013, [3] K. Sengupta JSSC 2012, [4] J. Grzyb JSSC 2013, [5] D. Shim VLSI 2011, [6] E. Öjefors ISSCC 2011

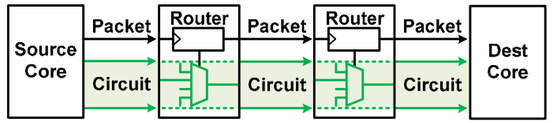
Performance Comparison Table

Paper No: 16.1

A 340mV-to-0.9V 20.2Tb/s Source-Synchronous Hybrid Packet/Circuit-Switched 16×16 Network-on-Chip in 22nm Tri-Gate CMOS

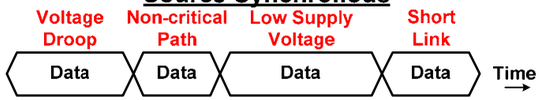
G. Chen, M. Anders, H. Kaul, S. Satpathy, S. Mathew, S. Hsu, A. Agarwal, R. Krishnamurthy, S. Borkar, V. De
Intel Corporation, Hillsboro, OR

Motivation



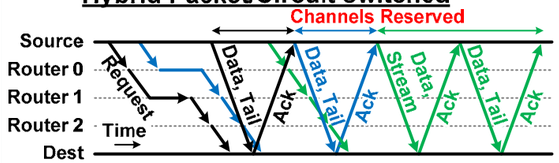
- Energy-efficient NoCs shift power budget from communication toward computation

Source-Synchronous



- Support more heterogeneity + V_{DD}/clock domains
- Lower clock and data synchronization power
- Adapts to delay imbalances → variation tolerant

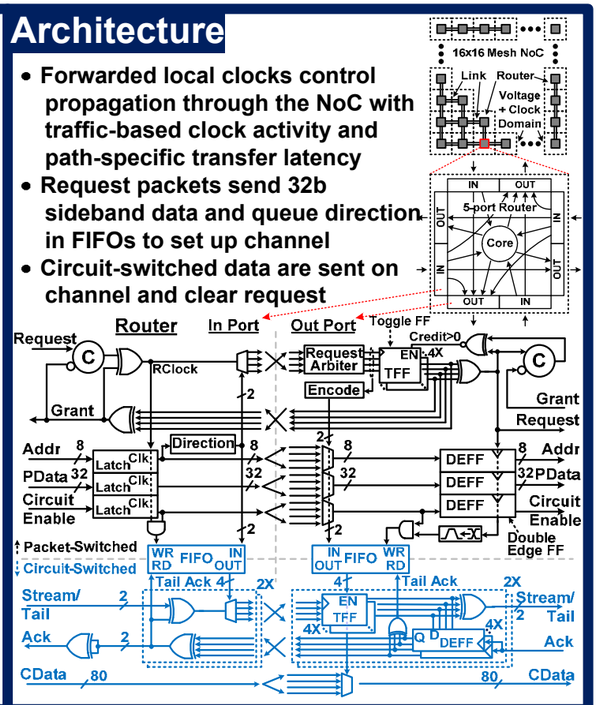
Hybrid Packet/Circuit-switched



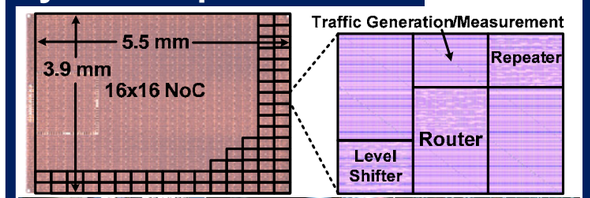
- Data storage removal → High energy efficiency
- Parallel channel setup + data → High throughput

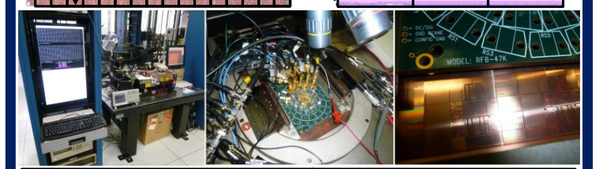
Architecture

- Forwarded local clocks control propagation through the NoC with traffic-based clock activity and path-specific transfer latency
- Request packets send 32b sideband data and queue direction in FIFOs to set up channel
- Circuit-switched data are sent on channel and clear request



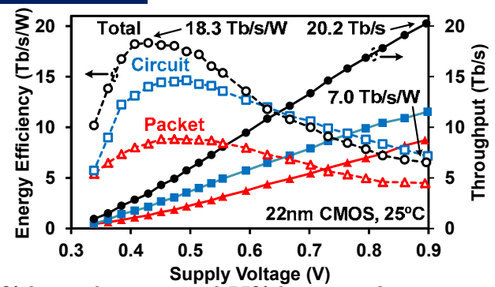
System Implementation



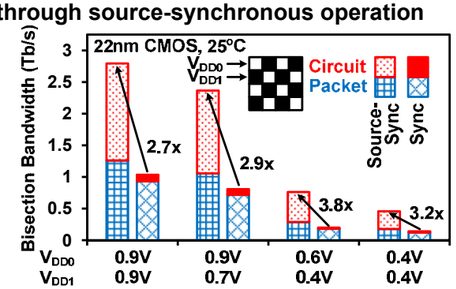


Process, Nom. V_{DD}	22nm Tri-gate, 0.9V
Equivalent NoC Area	13mm x 13mm
NoC Topology	256-node 16x16 Mesh
Interconnect	855µm, 112b data
Throughput	20.2Tb/s
Bisection Bandwidth	2.8Tb/s
Peak Energy Efficiency	18.3Tb/s/W @ 430mV
Power / Router	363µW @ 340mV

Verification



- 62% lower latency and 55% increase in energy efficiency to 7.0Tb/s/W with circuit switching
- 93% lower circuit-switched latency at 407ps/hop through source-synchronous operation



Paper No: 5.7

A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep

C. Tokunaga, J. Ryan, C. Augustine, J. Kulkarni, Y. Shih, S. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. Khellah, J. Tschanz, V. De
Intel Corporation, Hillsboro, OR

Motivation

Demonstrate energy-efficient, wide-voltage operation of a graphics processing core:

Leakage Reduction

- Leakage reduction using power gating with state-retention structures
- Active, digital retention clamp for sleep mode leakage reduction

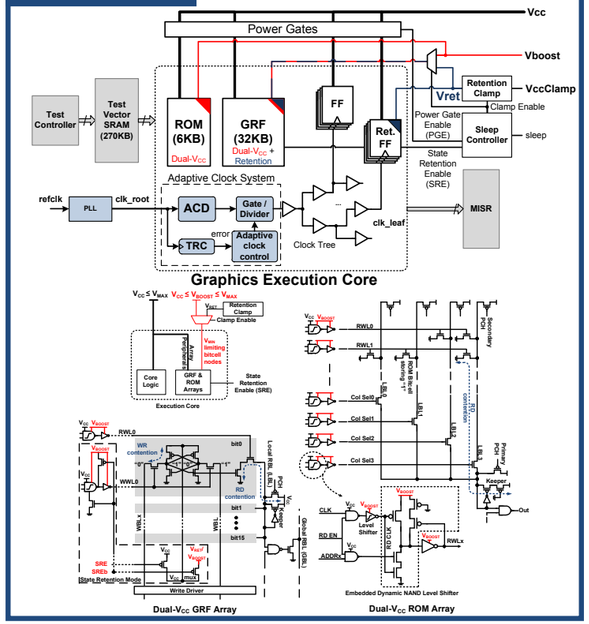
Adaptive and Resilient Circuits

- Voltage guardband reduction with timing monitors and adaptive clock distribution

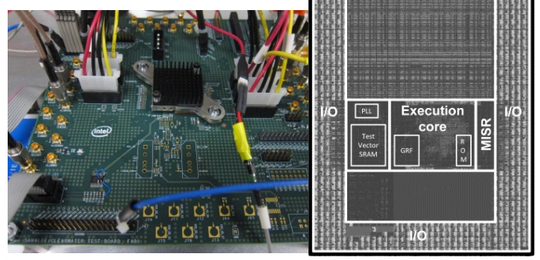
V_{MIN} Reduction

- Array V_{MIN} reduction using selective-boosting techniques in register file and ROM arrays

Overview

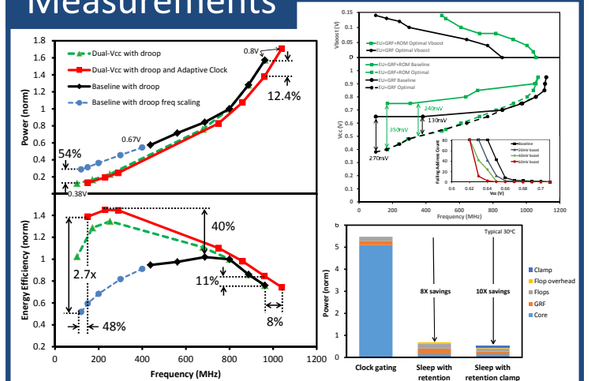


Implementation



Technology 22nm, 9-metal layer, tri-gate high-K/MG CMOS	
Area: testchip die	4.0 x 5.8 mm^2
Area: core + test	2.6 x 1.3 mm^2
Core transistor count	22.8M
Target voltage, frequency	0.7V, 800MHz
Retention sequentials	14,411
Package	FCBGA13 951

Measurements



- Retention clamp demonstrates leakage savings in sleep mode from 4X to 20X.
- Selective boosting provides V_{MIN} reduction of 270mV for the dual-Vcc GRF, and up to 350mV for the ROM.
- Dual-V_{CC} and adaptive clocking techniques improves energy efficiency up to 2.7X at low voltage, with peak energy efficiency gain of 40%.

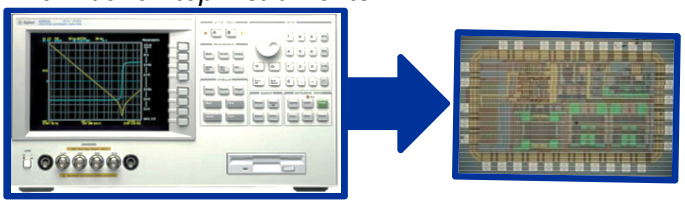
Paper No. : 17.4

CMOS impedance analyzer for nanosamples investigation operating up to 150MHz with sub-aF resolution

G.Ferrari, D.Bianchi, A.Rottigni and M.Sampietro
DEIB, Politecnico di Milano, P.za L. da Vinci32, 20133 Milano, Italy

Motivation

From bench-top instruments…



… to custom instrument-on-chip

- Compact & multichannel systems
- Low cost (standard CMOS technology)
- Input MOSFETs and connections tailored to match the small capacitance of micro- & nano-samples

CMOS Impedance Analyzer

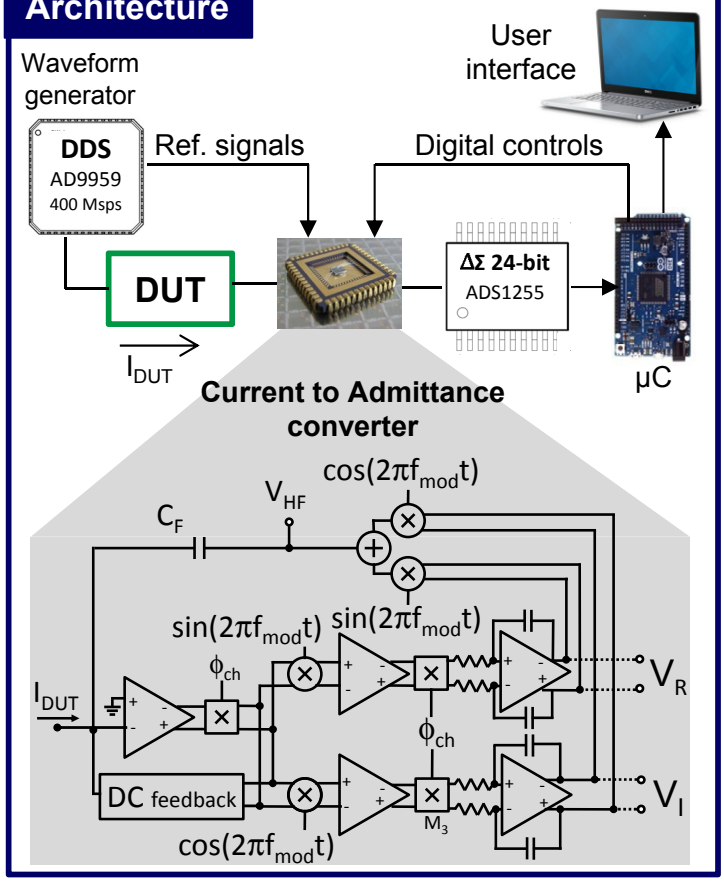
Features:

- Combination of chopping and modulation
- Capacitive feedback
- Real & Imaginary outputs

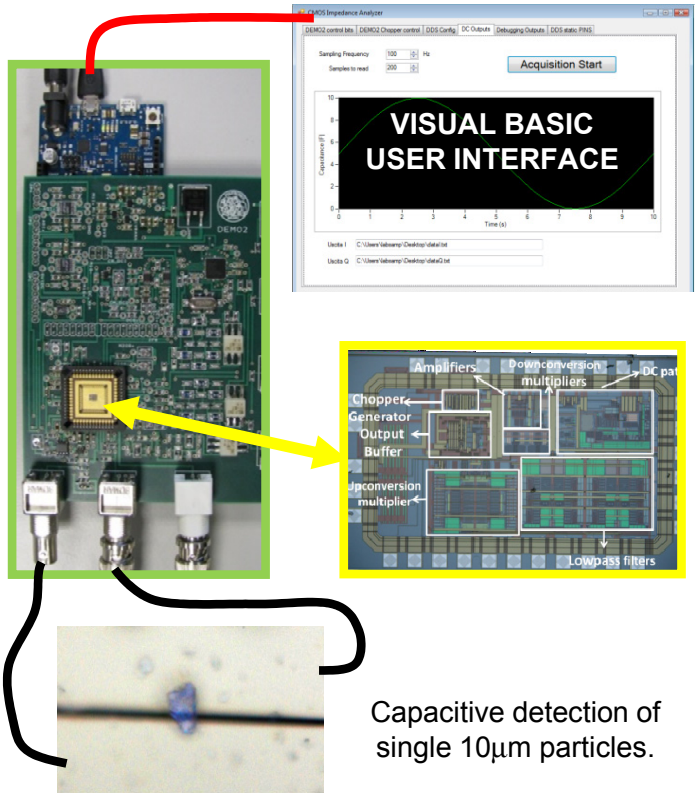
Benefits

- Wide operating frequency range: 1kHz–150MHz
- Low noise: 0.3aF resolution (100kHz to 100MHz)
- No off-chip processing is required

Architecture

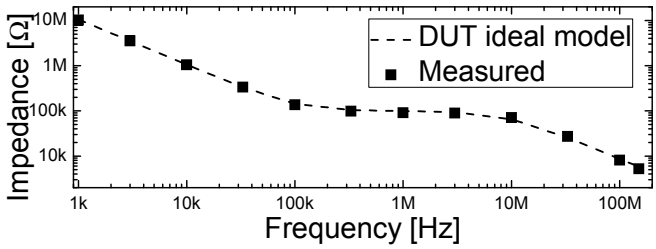


System Implementation

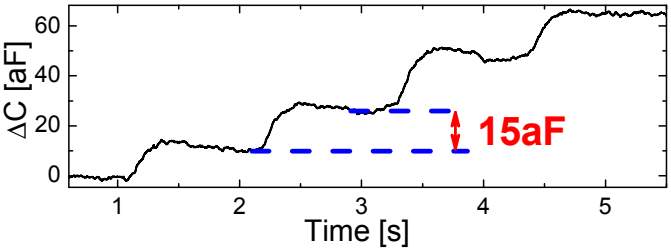


Capacitive detection of single 10μm particles.

Verification



Impedance spectrum of a known network connected as DUT to the input of the chip.



Capacitance variation measured for V_X=1V, f_{mod}= 1MHz and bandwidth BW=10Hz

Paper No. : 18.1

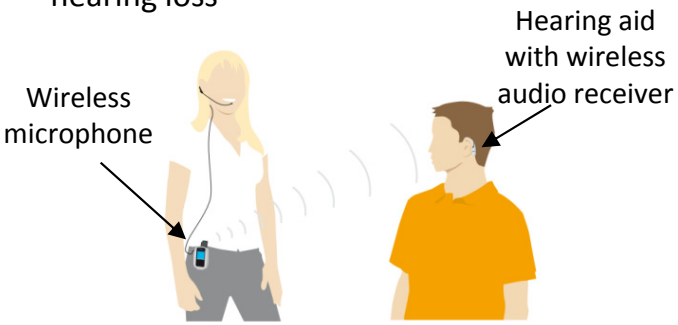
A 1V 3mA 2.4GHz wireless digital audio communication SoC for hearing aid applications in CMOS 0.18µm

Amre El-Hoiydi[1], François Callias[1], Yves Oesch[1], Christoph Kuratli[2], Robert Kvacek[3]

[1]Phonak Communications, Murten, Switzerland, [2]EM Microelectronic–Marin, Marin, Switzerland, [3]ASICentrum, Prague, Czech Republic

Motivation

Improving speech understanding in noise and over distance for persons with hearing loss



Digital system @ 2.4 GHz

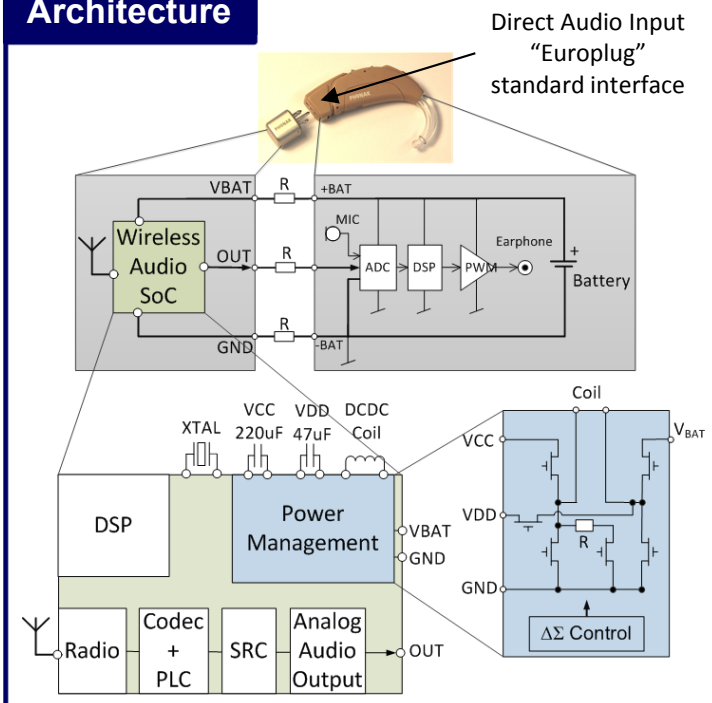
Benefits:

- Audio quality, privacy
- Usage simplicity (no frequency planning)
- World wide operation

Challenges:

- Low current consumption: <3mA@1.2V
- Constant current in the audible freq. band

Architecture



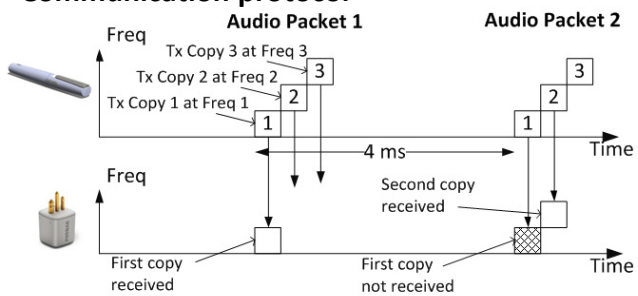
Power management avoids that radio current bursts cause audible ripple across the GND contact resistance.

System Implementation

Wireless Microphones

Receivers

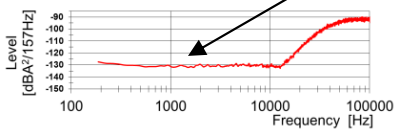
Communication protocol



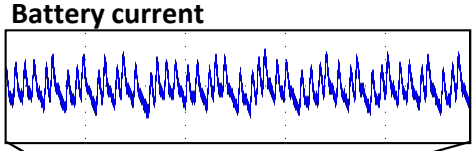
Verification

No audible noise in the audible frequency band

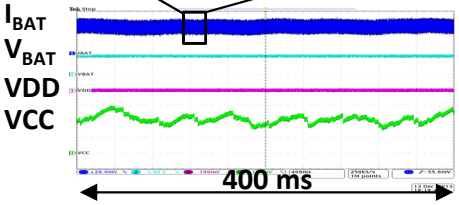
Spectrum of battery current

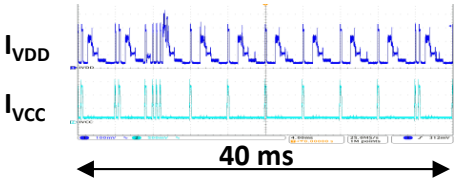


Battery current



Average battery current of 2.7 mA



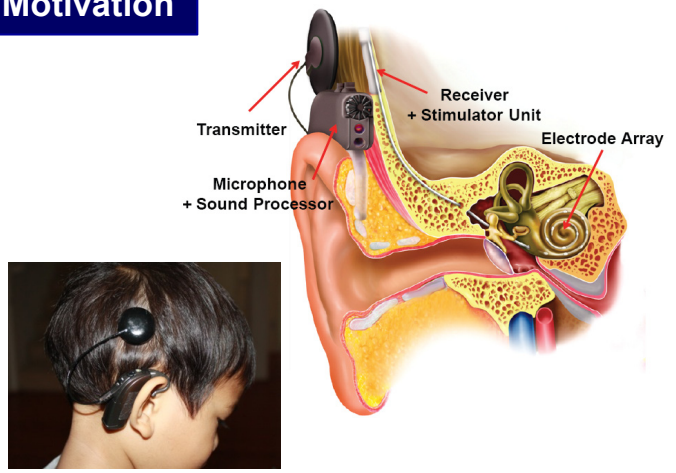


Paper No. : 18.2

A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18µm HVCMOS

Marcus Yip[1], Rui Jin[1], Nathan Ickes[1], Hideko Heidi Nakajima[2,3], Konstantina M. Stankovic[2,3], and Anantha P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, [2]Harvard Medical School, [3]Massachusetts Eye and Ear Infirmary

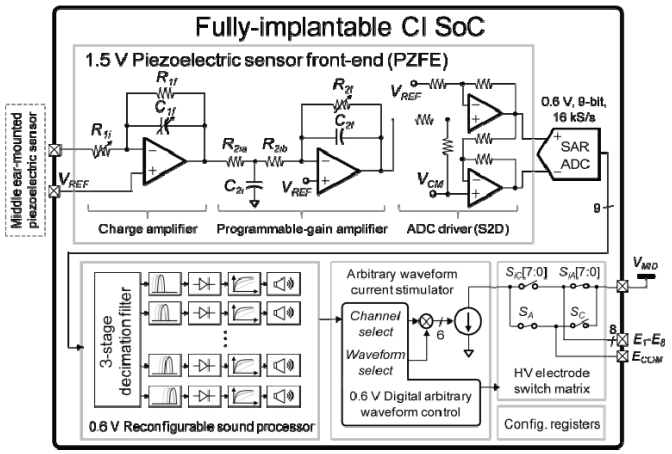
Motivation

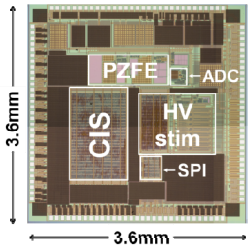


- Conventional cochlear implants (CIs) restore hearing for individuals with profound hearing loss
- CIs today rely on an external unit (to pick up and encode sound) which can be cumbersome, raises social stigma, and limits usage in water

A fully-implantable (i.e., internalized & invisible) solution is highly desirable

Architecture





0.18µm HVCMOS

- Middle-ear mounted piezoelectric sensor provides implantable acoustic sensing
- Reconfigurable digital sound processor enables system power scalability
- Arbitrary waveform neural stimulator provides 20-30% stimulation power savings

System Implementation

- SoC is tested by mounting the piezoelectric sensor on a human cadaveric specimen
- Sound is generated in the ear canal, and SoC outputs are compared against the measured umbo velocity and ear canal pressure

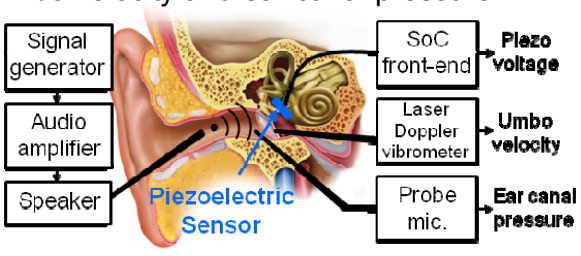
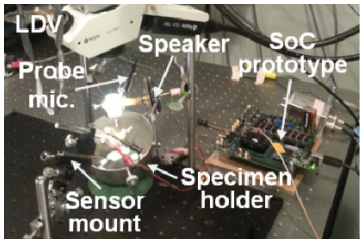
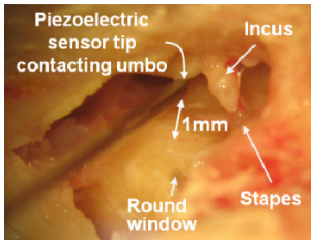


Diagram of the test setup with a fresh previously frozen human cadaveric specimen.

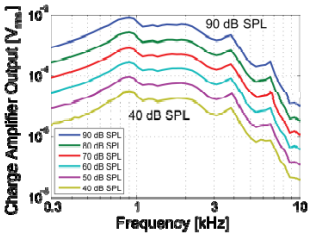


Photograph of test setup.

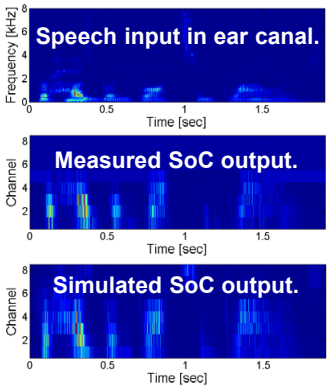


Close-up of human cadaveric middle ear.

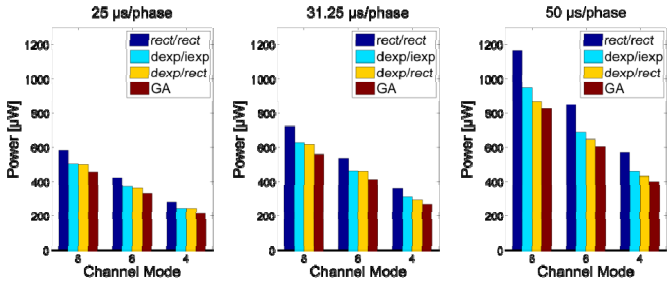
Verification



Frequency response of the mounted sensor and SoC charge amplifier for input sound levels from 40 to 90 dB SPL.



Spectrograms of the sentence “her husband brought some flowers”.



Measured neural stimulator power. Power savings is achieved by changing the waveform.

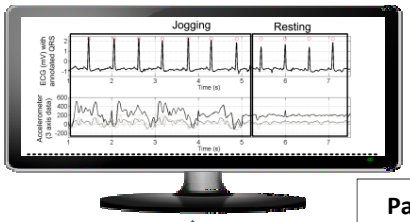
Paper No. : 18.3 and 10.6

Biomedical Wireless Sensor Platform Comprising Multi-Parameter Signal Acquisition SoC and 2.4 GHz Bluetooth Smart / Zigbee / IEEE 802.15.6 Personal Area Networks Radio

M. Konijnenburg, C. Bachmann, N. van Helleputte, G. van Schaik, B. Busze, M. Konijnenburg, Y. Zhang, J. Stuyt, M. Ashouei, G. Dolmans, T. Gemmeke, H. Kim*, J. Pettine, D. Jee*, A. Breeschoten, A. Morgado*, T. Torfs*, R. F. Yazicioglu*, H. de Groot, C. van Hoof*
imec – Holst Centre, Eindhoven, The Netherlands
*imec – Leuven, Belgium

Motivation

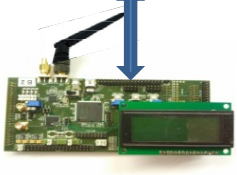
- **Energy-efficient, multi-sensor biomedical data acquisition with on-chip filtering and processing**
- **Low power, multi-standard wireless communication**



Paper 18.3

Person
3-lead ECG
Respiration
Accelerometer
Temperature

Biomedical SoC
Multi-sensor support
Hardware Motion Artefact Reduction
Matrix-multiply accelerator

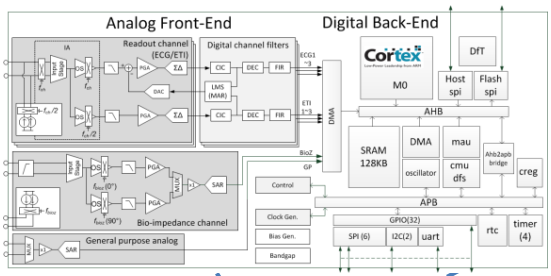


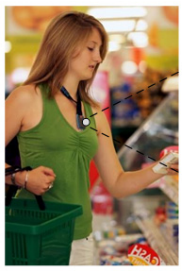
Paper 10.6

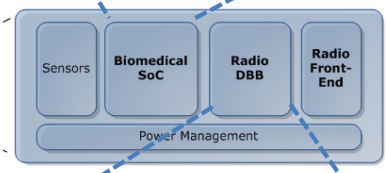
2.4 GHz PAN Radio Digital Baseband & Radio Front-End*
* [Y.-H. Liu et al., ISSCC 2013]

Commercial Device & SW App

Architecture

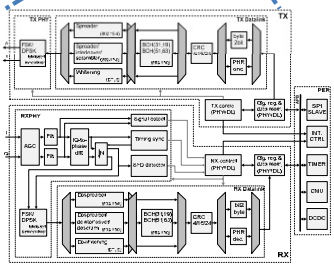






PAN Digital Baseband
Physical layer (PHY)
- Automated gain control
- Synchronization
- Mod./Demodulation

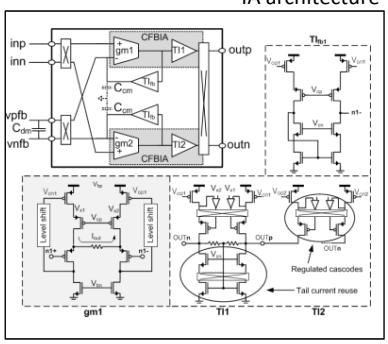
Datalink (DL)
- Spreading, interleaving, scrambling
- Forward error correction & CRCs
- MAC / SW protocol support



System Implementation

Biomedical SoC

IA architecture



Matrix operations accelerator

Supported operations:
- B = A · A^T
- A = B·A
- E = B·E
- A = A-E
- ICA matrix operation with contrast function
- $E = \left[\frac{\sum_{n=1}^{ns} a_{in}}{ns}\right]$

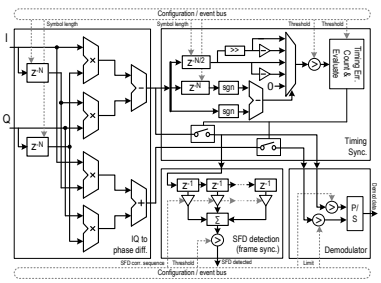
$A = \begin{bmatrix} a_{11} \dots a_{1s} \\ \vdots \\ a_{cs} \dots a_{cs} \end{bmatrix}$, $1 \le c \le 4$, $1 \le s \le 5120$

$B = \begin{bmatrix} b_{11} \dots b_{1c} \\ \vdots \\ b_{c1} \dots b_{cc} \end{bmatrix}$, $1 \le c \le 4$

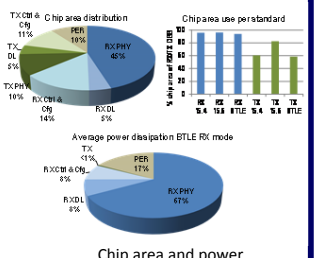
$E = \begin{bmatrix} e_1 \\ \vdots \\ e_c \end{bmatrix}$, $1 \le c \le 4$

		Cortex M0	Accelerator	Saving Factor
Cycles	M cycles	2.7	0.5	6.0
Power	(uW/MHz)	362.4	188.1	1.9
Energy	(uJ)	978.5	84.6	11.6

PAN Digital Baseband



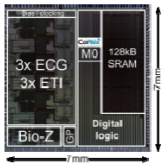
RX PHY: Low complexity synchronization and demodulation



Chip area and power consumption distribution

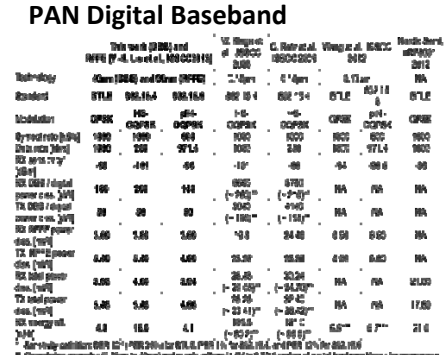
Verification

Biomedical SoC

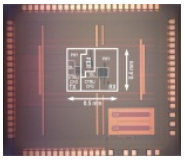


Data collection (2CH ECG+ETI and bioZ)	183µW (AFE) 112µW (DBE) **295µW (total)**
Multi-sensor application (2CH ECG+ETI, bioZ, and accelerometer data collection + MAR + R-peak detection)	183 µW (AFE) 191 µW (DBE) **374 µW (total)**

PAN Digital Baseband



BTLE radio link with PAN radio



PAN DBB 40nm die photo

Paper No. : 20.5

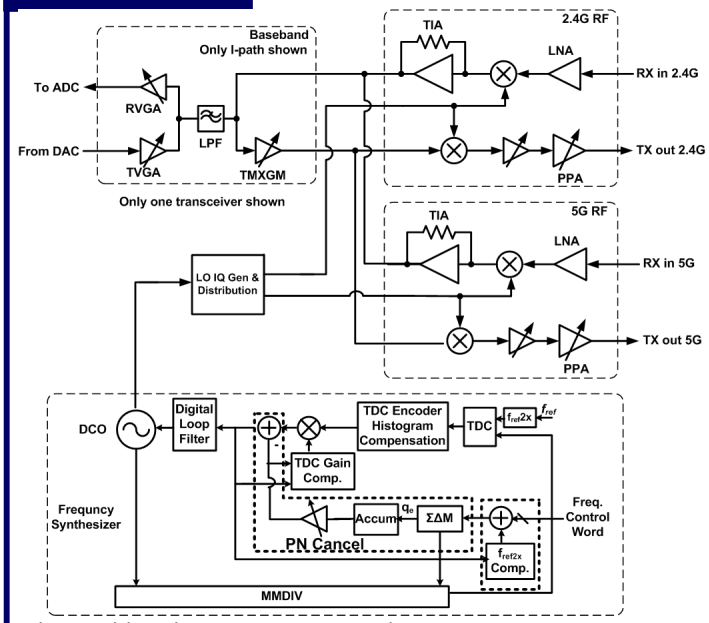
A 40nm Dual-Band 3-Stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s Over-the-Air Throughput

Ming He, Renaldi Winoto, Xiang Gao, Wayne Loeb, David Signoff, Wai Lau, Yuan Lu, Donghong Cui, Kun-Seok Lee, Sai-Wang Tam, Philip Godoy, Yung Chen, Sanghoon Joo, Changhui Hu, Arvind Anumula Paramanandam, Xiaoyue Wang, Chi-Hung Lin, Li Lin
Marvell, Santa Clara, CA

Motivation

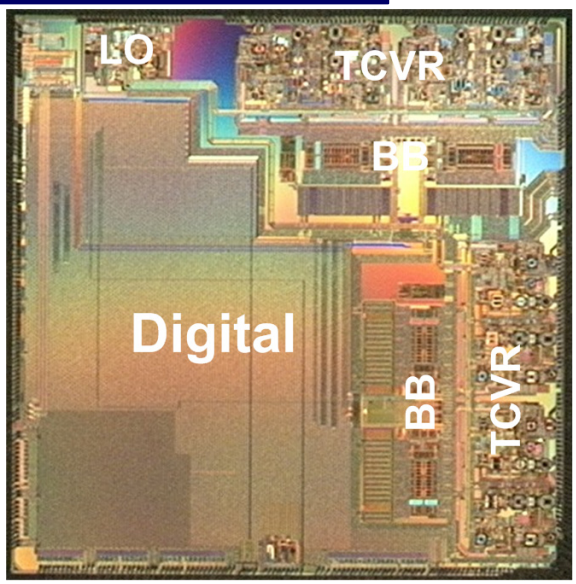
- IEEE 802.11ac provides substantially improved throughput and range, compared to existing 802.11a/b/g/n WLAN standards
- But wide signal BW (up to 80MHz) and high-density modulation (up to 256-QAM) leads to significant challenges in all aspects of RF transceiver design
- This demonstration will showcase a dual-band 3-stream 802.11a/b/g/n/ac MIMO 40nm CMOS SoC, which achieves an EVM floor of -37dB and an over-the-air IP throughput of 1.1Gbps.

Architecture



The Dual-band RF transceiver employs
- An all digital Frac-N PLL with FoM of -244dB
- A wideband low-impedance bias that minimize pre-PA driver memory effect
- A dual-band receiver with 3dB/4.3dB NF
- 5th-order Chebyshev LPF with constant-Gm bias and pre-distorted filter coefficient for up to 80MHz BW support

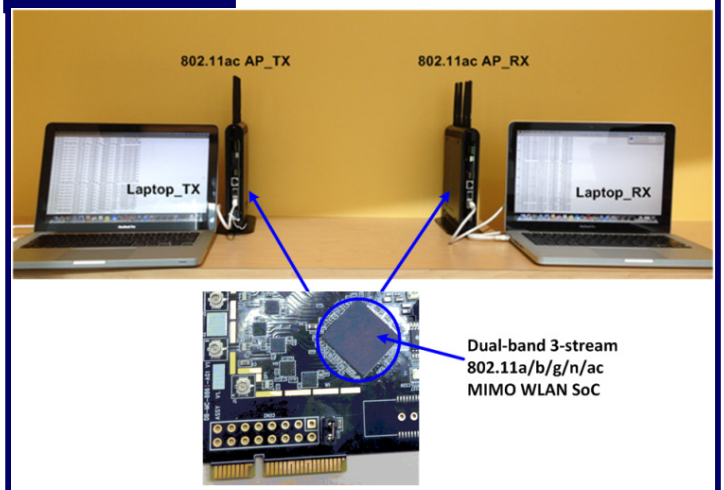
System Implementation



The 40nm CMOS SoC integrates
- Dual-band RF transceivers
- Data converters
- Digital circuits, including

-Digital physical layer
- Media access controller
- PCI Express Gen-2 interface

Verification



A complete dual-band 3-stream 802.11a/b/g/n/ac MIMO WLAN SoC platform (AP) is built and will be demonstrated.
- The SoC is mounted on a mini PCIE card, which is installed to the AP

-Traffic generator will be running on Laptop_TX and data packets will be sent through AP_TX
- AP_RX will receive data over the air and pass it to Laptop_RX
- Data throughput of both directions will be shown on the laptops
- TX EVM and mask could also be demonstrated

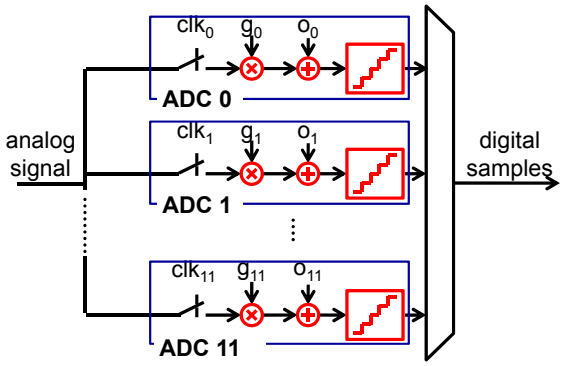
Paper No. : 22.5

A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS

N. Le Dortz[1,2], J-P. Blanc[1], T. Simon[1], S. Verhaeren[1], E. Rouat[1], P. Urard[1], S. Le Tual[1], D.Goguet[1], C. Lelandais-Perrault[2], P. Benabes[2]

STMicroelectronics[1], Supelec[2]

Motivation



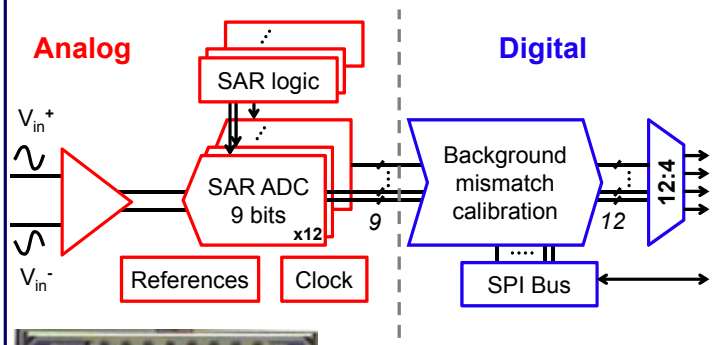
Increasing demand of **high speed ADCs** for high data rate communication systems (e.g. broadband satellite receivers)

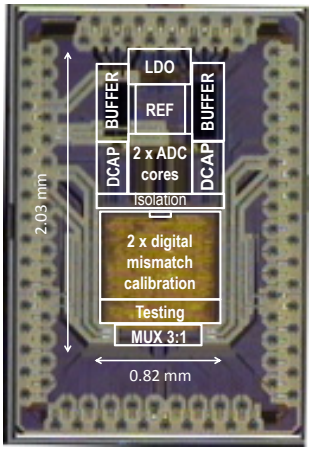
Time-interleaved ADCs achieve
- High sampling rate
- Moderate resolution

The **mismatches** between the converters limit the performances
- Spurious tones
- Increased noise
- Decreased SFDR

Calibration required to remove mismatch effects

Architecture





0.83mm² 1.6GS/s 9b TIADC in ST CMOS 40nm

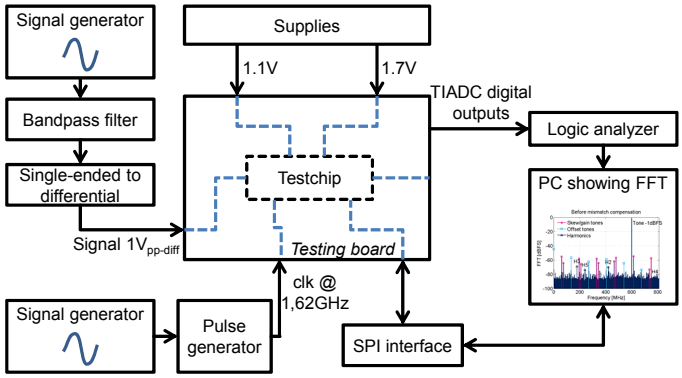
Analog/Digital co-design

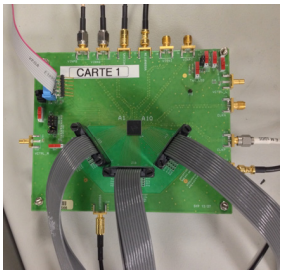
Background digital calibration of
- Offset mismatch
- Gain mismatch
- Skew mismatch

Decreased development time
- No feedback to analog
- High level synthesis for digital calibration

Scalable & reusable architecture

System Implementation

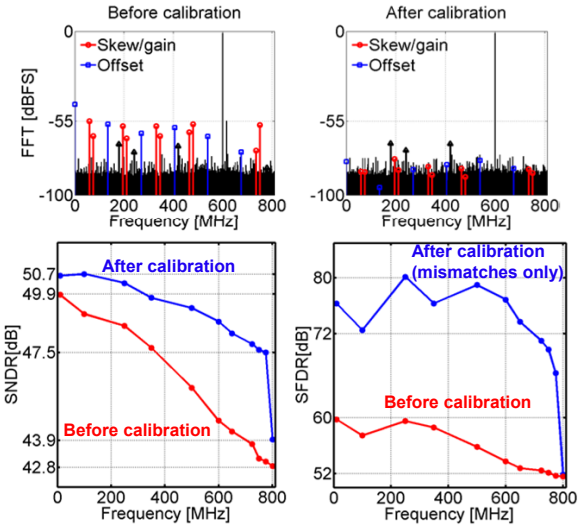




PCB:
- Packaged chip
- Interface with logic analyzer
- Clock & signal inputs
- SPI port
- Calibration ON/OFF switch

Performance analysis:
- Samples acquired by logic analyzer
- Real-time FFT on a PC

Verification



	Janssen2013	Doris2011	Stepanovic2011	This work
Technology	65nm	65nm	65nm	**40nm**
Sampling rate [GS/s]	3.6	2.6	2.8	**1.6**
Mismatch tones [dBFS]	50	55	60	**70**
SFDR[dBFS]	50	55	55	**62**
THD [dB]	-55	-58	-55	**-58**
SNDR [dB]	47	49	48	**48**
Power [mW]	795	480	44.6 (1)	**93**
FOM [fJ/conv]	1207	801	76 (1)	**283**
Area [mm²]	7.4	5.1	0.63 (1)	**0.83**

(1)without references and buffer

Best mismatch calibration published

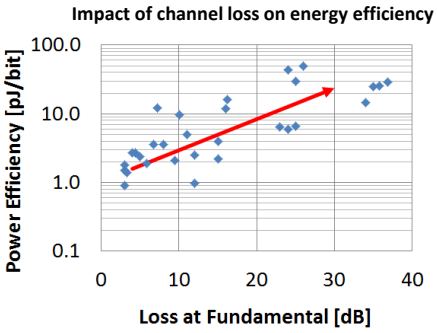
Paper No. : 26.2

A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS

James Jaussi[1], Ganesh Balamurugan[1], Sami Hyvonen[1], Tzu-Chien Hsueh[1], Tawfiq Musah[1], Gokce Keskin[1], Sudip Shekhar[2], Joseph Kennedy[1], Shreyas Sen[1], Rajesh Inti[1], Mozhgan Mansuri[1], Michael Leddige[1], Bryce Horine[1], Clark Roberts[1], Randy Mooney[1], Bryan Casper[1]
[1]Intel, [2]University of British Columbia

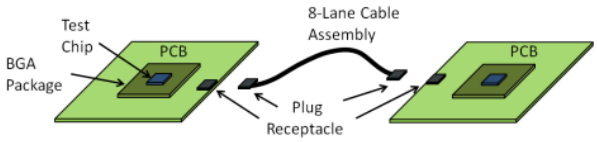
Motivation

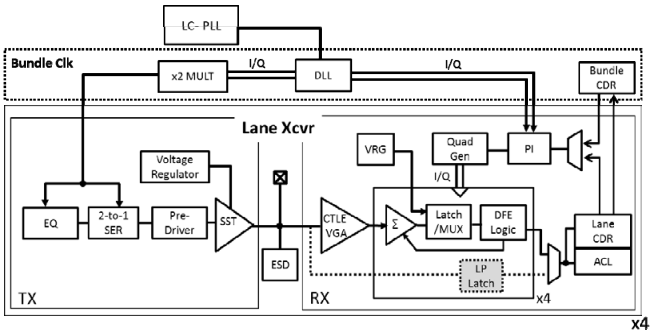
Serial I/O bandwidth demand continues to increase in many computing platforms



- Circuit-Channel co-design is necessary to optimize link energy efficiency
- Power-performance scalability enables unified PHY for multiple platforms

Architecture

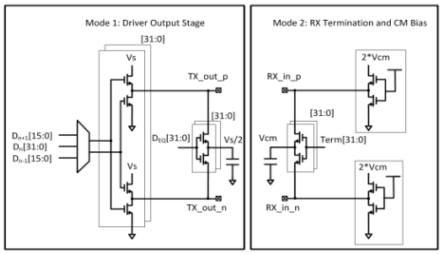




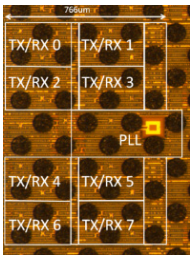
- Bundled clock architecture amortizes clocking power
- Bidirectional transceiver enables asymmetric TX/RX bandwidth
- Scalable CMOS clock distribution uses all-digital clock calibration based on asynchronous sampling
- Connector and cable improvements reduce channel loss

System Implementation

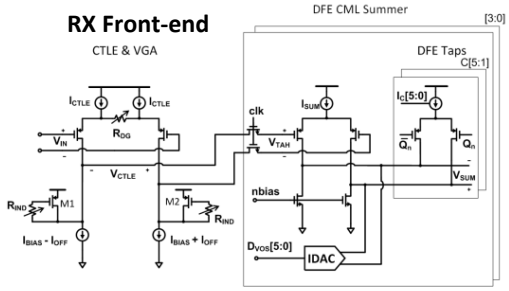
Configurable SST Driver



22nm CMOS



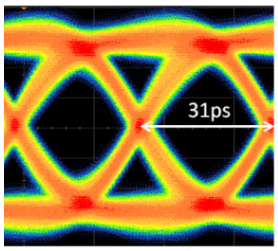
RX Front-end



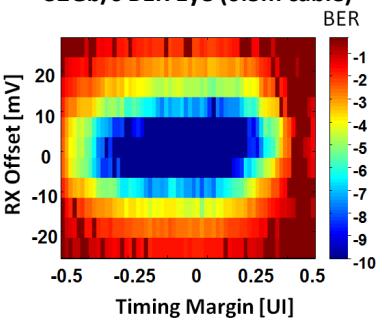
- TX: All-NMOS SST with differential equalization
- RX: CTLE with active inductor + 6-tap configurable DFE
- Baud-rate CDR with reduced comparator count
- Additional simple all-digital RX for ultra-low power operation when target channel loss is <12dB

Verification

32Gb/s TX Eye



32Gb/s BER Eye (0.5m cable)



Maximum data rate	32Gb/s	Maximum TX swing	630mV$_{pp\text{-}diff}$
Xcvr power efficiency**	5.7pJ/b	TX jitter	<540fs$_{rms}$
Xcvr area	0.08mm^2	Total loss @ 16GHz	16dB

**Includes all active circuits in a 4-lane bundle (excludes global PLL)

- **Demonstrated power-performance scalability from 1.0pJ/bit at 4Gb/s to 5.7pJ/bit at 32Gb/s**

Paper No. : 26.3

A Pin- and Power-Efficient Low-Latency 8-to-12Gb/s/wire 8b8w-Coded SerDes Link for High-Loss Channels in 40nm Technology

A. Singh[1], D. Carnelli[1], A. Falay[1], K. Hofstra[1], F. Licciardello[1], K. Salimi[1], H. Santos[1], A. Shokrollahi[1], R. Ulrich[1], C. Walter[1], J. Fox[2], P. Hunt[2], J. Keay[2], R. Simpson[2], A. Stewart[2], G. Surace[2], H. Cronie[3]

[1] Kandou Bus, Lausanne, Switzerland; [2] Kandou Bus, Northampton, United Kingdom; [3] Lausanne, Switzerland

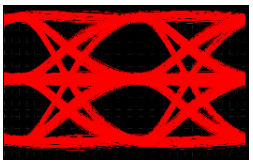
KANDOU BUS

Motivation

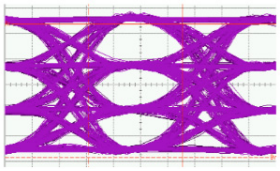
- Latest systems and standards require high bandwidth at better power efficiency
- Lower pin count is highly desirable
- Choice of coding and signaling scheme determines SNR and susceptibility to ISI

8b8w coding:
- 8-conductor electrical interface, with ternary signals on each conductor ('-1', '0', '+1')
- Each 8b data word mapped to a code word consisting of 2 '-1's, 2 '+1's, 4 '0's → permutations of {+1, +1, -1, -1, 0, 0, 0, 0}
- Receiver front-end detects 2 max. and 2 min. voltages to determine the code word, decoder recovers the 8b data word
- Highly efficient implementation of 8b8w encoder and decoder

8b8w



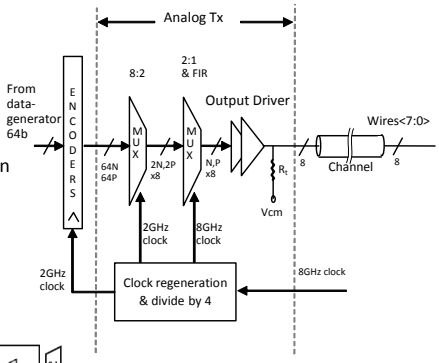
PAM-4

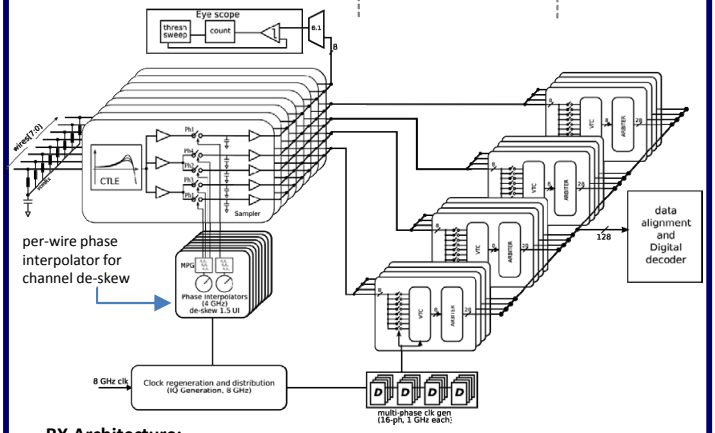


8b8w is a fully pin efficient ternary signaling scheme that gives better SNR compared with PAM-4.

Architecture

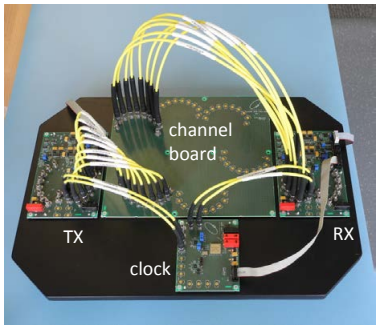
TX Architecture:
- 64b data encoded to 8b8w (P/N signals)
- 2-stage mux serialization
- 1 FIR post-tap for equalization





RX Architecture:
Joint EQ across the 8 wires followed by 16-phase time-interleaved voltage-to-time converters with arbitration logic to detect the two max (+1) and two min (-1) values on the wires

System Implementation

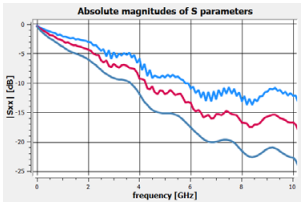


DUT:
Chip board with transceiver mounted as chip-on-board, I/O fan-out to 2x8 SMA connectors, SPI test interface, DAC-controlled power supplies

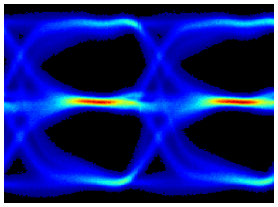
Channel:
Channel board with 3 sets of traces, for a total channel length of 369mm/556mm/792mm (Rogers RO4350B/RO4450F)

Clock:
custom clock PCB generating 4-8GHz differential clocks

Total channel IL of 3 test channels

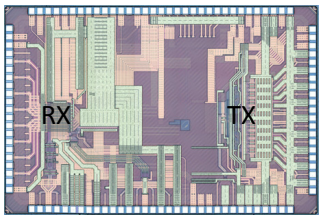


TX output waveform at 12Gb/s



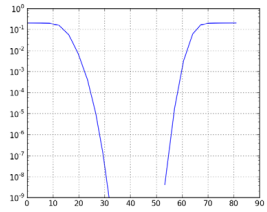
Verification

Chip micrograph



Technology	40nm CMOS GP, VDD=0.9V, 10M, DGO
Package	Wire bond (1.5-2.0 mm length), COB
Data Rate	8-12Gb/s/wire
Nominal Power	412mW
Energy Efficiency	4.29pJ/bit at 12Gb/s/wire
BER	$<8x10^{-15}$ at 12Gb/s/wire
64b encoder latency, area, power	0.5ns, 2000µm², 3mW
64b decoder latency, area, power	0.5ns, 1330µm², 4mW
Testability	Pattern generators (prbs31, prbs9), on-chip Eye Scope, error counters, SPI, analog test bus, test software
Per wire RX de-skew	1UI

BER bathtub plot at 12Gb/s/wire



	8b8w 8GTps	Differential 16GTps
Total, mW	316.61	504.53
Transfer rate	8	16
Bit width	8	4
pJ/bit	**4.95**	**7.88**

Measured energy efficiency: 8b8w vs. Differential at 64Gb/s BW

Paper No. : 30.2

Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption

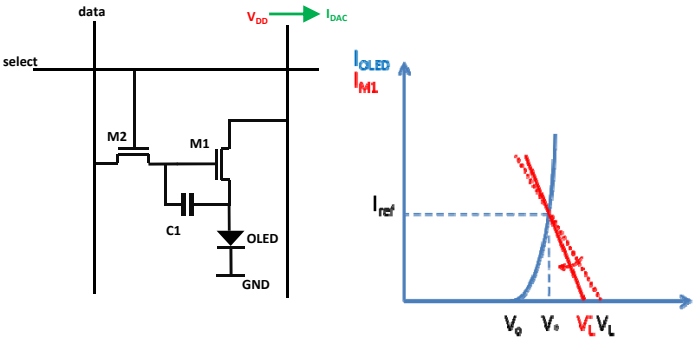
Jan Genoe[1,2], Koji Obata[3], Marc Ameys[1], Kris Myny[1], Tung Huei Ke[1],Manoj Nag[1], Soeren Steudel[1], Sarah Schols[1], Joris Maas[4],Ashutosh Tripathi[4], Jan-Laurens van der Steen[4], Tim Ellis[4],Gerwin H. Gelinck[4], Paul Heremans[1,2,4]

[1]imec, Leuven, Belgium, [2]KU Leuven, Leuven, Belgium,[3]Panasonic, Osaka, Japan, [4]Holst Centre/TNO, Eindhoven, The Netherlands

Motivation

Digital current driving moves the control of the OLED current in an AMOLED display from the pixel to the external silicon drivers. This yields:

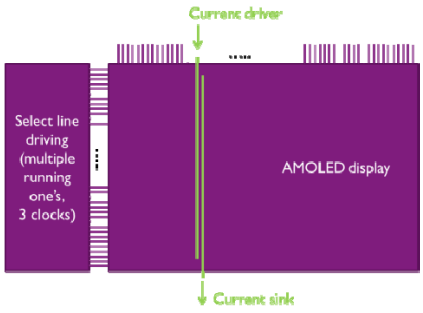
- Methods for accurate current calibration
- Compensation of mobility degradation, V_T non-uniformity and bias stress of the TFTs on the display backplane
- Linear response of the light output (PWM)
- Reduced power consumption in the backplane (TFT operated in the linear regime)
- Higher resolution (transistors operated in the linear regime can have downscaled channel length (L) as short channel effects are no longer relevant)

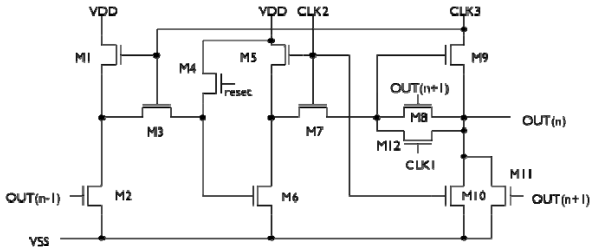


Architecture

Dedicated select line driver, embedding multiple active signals, has been designed to enable Pulse Width Modulation of the OLED current.

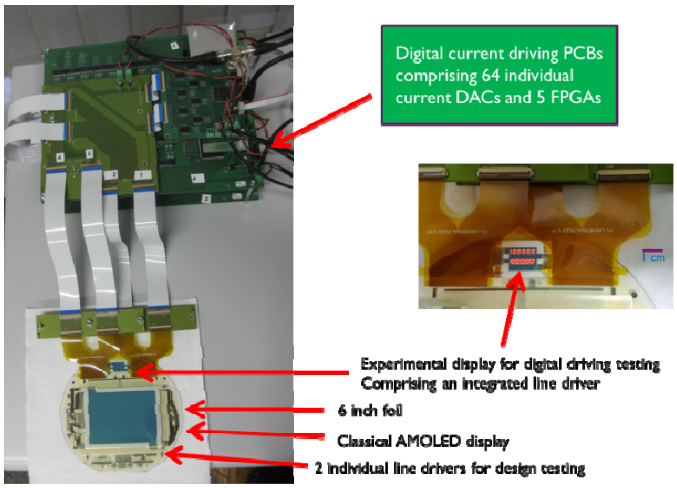
A 3-clock implementation avoided that two active signals would drive simultaneous a select line.





System Implementation

A 160*64 pixel AMOLED display (80µm*80µm pixels) has been realized on a flexible foil. The dedicated line driver has been implemented on the same foil. Both the backplane and the line-driver circuit have been implemented using amorphous IGZO TFTs. The current- and data-driving has been realized using discrete components on external PCBs.



Verification

The dedicated select line driving circuit on foil has been tested and has shown to be operational up clock frequencies beyond 360 kHz (see Shmoo Plot)